VIRUDHUNAGAR S.VELLAICHAMY NADAR POLYTECHNIC COLLEGE
(AUTONOMOUS),
(Affiliated to Directorate of Technical Education, Chennai – 25)
VIRUDHUNAGAR – 626 001.

SYLLABUS

DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING

N1 – SCHEME

(2019-2020 onwards)

OUTCOME BASED EDUCATION

Head of the Department **Principal**

VIRUDHUNAGAR S.VELLAICHAMY NADAR POLYTECHNIC COLLEGE
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VIRUDHUNAGAR.

N1 - SCHEME

Regulations [MPEC SYSTEM]

(Implemented from 2019-2020)

Diploma in Electronics and Communication Engineering

1. Autonomy and Multi Point Entry and Credit System:

As per G.O Ms 1136 dated 20.11.92 our Institution has been granted Autonomous status from the academic year 1994–95.

The Students admitted for the I Term Engineering at this Institution in Multi Point Entry Credit System (MPEC) will study under Autonomous pattern.

2. Condition for Admission:

Condition for admission to the Diploma Courses shall be required to have passed in the S.S.L.C. Examination of the Board of Secondary Education, Tamil Nadu.

(Or)

The Anglo Indian High School Examination with eligibility for Higher Secondary Course in Tamil Nadu.

(Or)

The Matriculation Examination of Tamil Nadu.

(Or)

Any other Examination recognized as equivalent to the above by the Board of Secondary Education, Tamil Nadu.

Note: In addition, at the time of admission the candidate will have to satisfy certain minimum requirements, which may be prescribed from time to time.

3. Admission to Second year (Lateral Entry):

A pass in HSC (Academic) or (Vocational) Courses mentioned in the Higher Secondary Schools in Tamil Nadu affiliated to the Tamil Nadu Higher Secondary Board with eligibility for University Courses of study or equivalent examination and should have studied the following subjects.

Sl. No.	Courses	H.Sc. Academic	H.Sc. Vocational	
		Subjects Studied	Subjects Studied	
			Related Subjects	Vocational Subjects
1.	All the Regular Diploma Courses	Physics, Chemistry & Mathematics/Biology (Botony and Zoology)	Maths / Physics / Chemistry	Related Vocational Subjects Theory & Practical
2.	Diploma Course in Modern Office Practice	English & Accountancy English & Elements of Economics English & Elements of Commerce	English & Accountancy, English & Elements of Economics, English & Management Principles & Techniques, English & Typewriting	Accountancy & Auditing, Banking, Business Management, Co-operative Management International Trade, Marketing & Salesmanship, Insurance & Material Management, Office Secretary ship.

- For the diploma programmes related with Engineering/Technology, the related / alternate courses prescribed along with Practical may also be taken for arriving the eligibility.
- Programme will be allotted according to merit through counseling by the Principal as per communal reservation.
- *Candidates who have studied Commerce Subjects are not eligible for Engineering Diploma Courses.*

4. Age Limit : No Age Limit

5. Medium of Instruction : English

6. Courses of Study and Curriculum Outline:

The Courses of study shall be in accordance with the curriculum prescribed by the Autonomous Academic Board from time to time, both in Theory and Practical. The curriculum outline is given in Annexure–I.

7. Description of the Programme:

The Programme for the Full Time Diploma in Engineering & Technology / MOP shall extend over a period of three academic years, consisting of six terms. Each Term will have 15 weeks duration of study.

The Curriculum for all the Six Terms of Diploma Programme have been revised and revised curriculum is applicable for the candidates admitted from 2019–2020 academic year onwards.

8. Requirements of Examination and Attendance:

The Examination shall be conducted at the end of each term by the Autonomous body affiliated to the State Board of Technical Education and Training, Tamilnadu.

A Candidate will be permitted to appear for the Autonomous End Examinations only if he/she secures minimum 80% of attendance in the term concerned.

If the candidate does not appear for at least one of the regular courses in the End Examination, he/she has to attend the same term in the next academic year.

9. Eligibility for the Award of Diploma:

No candidate shall be eligible for the award of Diploma unless he/she has undergone the prescribed programme of study for a period of not less than **three academic years** in the Institution, when joined in First Year and **two academic years** if joined under Lateral Entry scheme in the second year and passed the prescribed examination. The minimum and maximum periods for completion of Diploma Programme are as given below.

Diploma Courses	Minimum Period	Maximum Period
Full Time	**3 Years**	**6 Years**
Full Time (Lateral Entry)	**2 Years**	**5 Years**

10. Autonomous End Examinations:

Autonomous End Examinations in all Programme of all the terms under the scheme of examinations will be conducted at the end of each term both in theory and practical. The internal assessment marks for all the courses will be awarded on the basis of continuous internal assessment earned during the term concerned. For each course, 25 Marks are allotted for internal assessment and 75 Marks are allotted for End Examination.

11. Continuous Internal Assessment:

I) THEORY

The Continuous Internal assessment marks for a total of 25 Marks, which are to be distributed as follows:

Test	-	**10 Marks**
Assignment / Drawing Plate	-	**10 Marks**
Course Attendance	-	**5 Marks**
Total		**25 Marks**

(i) Test **10 Marks**

Two Periodical Tests each of two hours duration for total of 50 Marks each and Model Examination for three hours duration for 75 Marks are to be conducted. The average of two periodical tests (PT) is to be taken for 5 Marks and Model Exam to be taken for another 5 marks. The periodical test mark and model exam marks are to be converted to five marks and awarded with the next higher integer if there is any fraction.

Total test marks (5 + 5) = 10 Marks

TEST	SYLLABUS	MAXIMUM MARKS	DURATION	WHEN TO CONDUCT
Periodical Test – I	I & II Unit	50	2 Hrs.	30 working days from Reopening
Periodical Test – II	III & IV Unit	50	2 Hrs.	30 working days from first periodical test
Model Exam	All Units	75	3 Hrs.	After last working day

(a) [i] Question Paper Pattern for Periodical Test – I & Test – II (First Year)

With No Choice

Part – A	4 Questions x 2 Marks	-	8 Marks
Part – B	4 Questions x 3 Marks	-	12 Marks
Part – C	6 Questions x 5 Marks	-	30 Marks
		Total	50 Marks

[ii] Question Paper Pattern for Periodical Test – I & Test – II (Engineering)

With No Choice:

Part – A	4 Questions x 2 Marks	-	8 Marks
Part – B	4 Questions x 3 Marks	-	12 Marks
Part – C	3 Questions x 10 Marks	-	30 Marks
		Total	50 Marks

[iii] Question Paper Pattern for Periodical Test – I & Test – II

(Modern Office Practice)

With No Choice:

Part – A	4 Questions x 5 Marks	-	20 Marks
Part – B	2 Questions x 15 Marks	-	30 Marks
		Total	50 Marks

(b) Question Paper Pattern for Model Exam:

(First Year, Engineering & Modern Office Practice)

As per Syllabus Book

(ii) Assignment **10 Marks**

For each course, three Assignments are to be given each for 10 Marks and the total marks scored should be converted to 10 Marks and awarded with the next higher integer if there is any fraction.

(iii) Course Attendance **5 Marks**

Award of marks for course attendance to each Theory / Practical Course / Project Work and Seminar will be as per the range given below.

Attendance mark reference table

Range of Attendance (%)	Marks
80% - 83%	1
84% - 87%	2
88% - 91%	3
92% - 95%	4
96% - 100%	5

(iv) Total

The Attendance (5 Marks), Assignment (10 Marks) & Test Marks (10 Marks) should be added and the Continuous Internal assessment marks for a total of 25 Marks is arrived.

II) PRACTICAL / DRAWING

The internal assessment mark calculation for Practical courses is given as follows:-

a) Observation and Exercise	:	10 Marks
b) Model Practical Examination	:	10 Marks
c) Attendance	:	5 Marks
Total	:	25 Marks

- After completion of each exercise, record should be submitted in the subsequent practical classes and marks awarded for observation should be carried over to record.
- The mark should be awarded for 10 in each exercise.
- The students have to submit the duly signed Bonafide record note book / file during the End Practical Examinations.
- All the experiments indicated in the syllabus should be completed and the same be given for final End Examinations.

Note: All the marks awarded for Assignments, Tests and Attendance should be entered in the course file / log book of the staff, who is handling the course. This is applicable to both Theory and Practical courses.

For Drawing

For drawing courses, 20 Marks should be awarded for each drawing plate. The total of all drawing plate marks should be converted to 10 marks and awarded with the next higher integer if there is any fraction.

12. Project Work and Seminar:

The students of all the Diploma Programmes have to do a Project Work and Seminar as part of the Curriculum and in partial fulfillment for the award of Diploma by the State Board of Technical Education and Training, Tamilnadu.

In order to encourage students to do worthwhile and innovative projects, every year prizes are awarded for the best three projects in department, institution wise, region wise and state wise. The selection of Project Work should be taken up in V Term of study.

The Project may be reviewed twice during 4th and 10th week of VI Term.

a) Internal assessment marks for Project Work and Seminar:

Project Review I & II (VI Term) (5+5)	:	10 Marks
Seminar I & II (5+5)/2	:	5 Marks
Project report	:	5 Marks
Attendance (Award of marks same as course pattern)	:	5 Marks
TOTAL	:	25 Marks

b) Mark Allocation for Project Work and Seminar in End Examination:

Viva Voce	:	25 Marks
Demonstration / Presentation	:	50 Marks
(The following Criteria components to be considered- Relevance of topic, Knowledge of methodology, Role of individual in the team, finding the Study etc.)		
TOTAL	:	75 Marks

A neatly prepared **PROJECT REPORT** as per the format has to be submitted by individual student during the Project work End Examination.

Selection of seminar topics should be based on Professional Ethics, Environmental Engineering and Management.

Proper record is **to be maintained for the two project reviews & seminars** and it should be preserved for two terms.

13. Academic Audit:

All Test Papers and assignment note books after getting the signature with date from the students must be kept in the safe custody in the Department for verification and audit for two terms.

14. Criteria for pass:

1. No candidate shall be eligible for the award of Diploma unless he/she has undergone the prescribed programme of study successfully and pass all the courses prescribed in the curriculum.

2. A candidate shall be declared to have passed the examination in a course if he/she secures not less than 40% in Theory courses and 50% in Practical courses out of the total prescribed maximum marks including both the Internal Assessment and the End Examination marks put together, subject to the condition that he/she has secured at least a **minimum of 30 Marks out of 75 Marks in the End Theory and a minimum of 35 Marks out of 75 Marks in the End Practical Examinations.**

15. Classification of successful candidates:

Classification of candidates who pass out the final examinations from April 2022 onwards (joined in first year 2019-2020) will be done as specified below.

First Class with Superlative Distinction

A Candidate will be declared to have passed in **First Class with Superlative Distinction** if he/she secures not less than 75% of the marks in all the courses and passes all the terms in the first appearance itself and passes all the courses within the stipulated minimum period of study without any break in study.

First Class with Distinction

A Candidate will be declared to have passed in **First Class with Distinction** if he/she secures not less than 75% of the aggregate of marks in all the terms put together and passes all the above terms except the I & II Term in the first appearance itself and passes all the courses within the stipulated minimum period of study without any break in study.

First Class

A Candidate will be declared to have passed in **First Class** if he/she secures not less than 60% of the aggregate marks in all terms put together and passes all the courses within the stipulated minimum period of study without any break in study.

Second class

All other successful candidates will be declared to have passed in **Second Class**.

16. Duration of a period in the Class Time Table:

The duration of each period of instruction is one hour and the total period of instruction hours excluding interval and lunch break in a day should be uniformly maintained as seven hours corresponding to seven periods of instruction (Theory & Practical).

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PROGRAMME: Diploma in Electronics and Communication Engineering

N1–SCHEME

ANNEXURE - I

LIST OF COURSES

I FOUNDATION COURSES

Course Code	Name of the course	Credits	Prerequisites
N1BE101	Communication English-I	2	-
N1BE102	Engineering Mathematics	5	-
N1BE103	Engineering Physics-I	3	-
N1BE104	Engineering Chemistry– I	3	-
N1BE105	Engineering Physics -I Practical	2	-
N1BE106	Engineering Chemistry -I Practical	2	-
N1BE107	Communication Skill Practical	3	-
N1BE108	Computer Application Practical	3	-
N1BE109	Communication English-II	2	N1BE101
N1BE110	Applied Mathematics	4	N1BE102
N1BE111	Engineering Physics –II	2	N1BE103
N1BE112	Engineering Chemistry-II	2	N1BE104
N1BE113	Engineering Physics -II Practical	2	N1BE105
N1BE114	Engineering Chemistry -II Practical	2	N1BE106
Total Credits		**37**	

II CORE COURSES

Course Code	Name of the course	Credits	Prerequisites
N1BE201	Engineering Graphics	5	-
N1BE202	Engineering Drawing	5	N1BE201
N1BE203	Workshop Practice	3	-
N1EC204	Electronic Devices and Circuits	6	N1BE111
N1EC205	Electrical Circuits and Instrumentation	6	N1BE110 & N1BE111
N1EC206	Communication Engineering	6	N1BE110 & N1EC204
N1EC207	Digital Electronics	5	N1EC204
N1EC208	Electronic Devices and Circuits Practical	3	N1BE113
N1EC209	Electrical Circuits and Instrumentation Practical	3	N1BE113
N1EC210	Industrial Electronics and Communication Engineering Practical	3	N1EC208
Total Credits		**45**	

III APPLIED COURSES

Course Code	Name of the course	Credits	Prerequisites
N1EC301	Programming in "C"	6	-
N1EC302	Industrial Electronics	5	N1EC204
N1EC303	Linear Integrated Circuits	4	N1EC204 & N1EC205
N1EC304	Advanced Communication Systems	6	N1EC206
N1EC305	Microcontroller	6	N1EC207
N1EC306	Very Large Scale Integration	5	N1EC207
N1EC307	Computer Hardware Servicing and Networking	6	N1EC205
N1EC308	Biomedical Instrumentation	6	N1EC205
N1EC309	Programming in "C" Practical	3	-
N1EC310	Integrated Circuits Practical	3	N1EC208
N1EC311	Advanced Communication Systems Practical	2	N1EC210
N1EC312	Microcontroller Practical	2	N1EC309 & N1EC310
N1EC313	Very Large Scale Integration Practical	2	N1EC310
N1EC314	Computer Hardware Servicing and Networking Practical	3	N1EC209 & N1BE108
N1EC315	PCB Design Practical	3	-
N1EC316	Project Work and Seminar	3	N1BE107
Total Credits		**65**	

IV DIVERSIFIED COURSES

Course Code	Name of the course	Credits	Prerequisites
N1EC401	CCTV & Security Systems Practical	2	N1EC304 & N1EC311
N1EC402	Home Appliances servicing and Arduino Programming Practical	3	N1EC209 & N1EC309
Elective Theory – I			
N1EC403 N1EC404 N1EC405	1. Digital Communication 2. Mobile Communication 3. Television Engineering	5	N1EC206 N1EC206 N1EC302
Elective Theory – II			
N1EC407 N1EC408 N1CO400	1. Embedded systems 2. Programmable Logic Controller 3. Nano and Solar Engineering	5	N1EC305 N1EC302 N1EC302
Elective Practical – I			
N1EC409 N1EC410 N1CO401	1. Embedded systems Practical 2. Programmable Logic Controller Practical 3. Nano and Solar Engineering Practical	3	N1EC309 & N1EC312 N1EC210 N1EC210
Total Credits		**18**	

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PROGRAMME: All Programme of Diploma in Engineering and Technology except

DMOP N1–SCHEME

MPEC SYSTEM

TOTAL CREDITS FOR THE COURSES 165

NAME OF THE COURSE	Credits	Percentage (%)
FOUNDATION COURSE	37	22.4
CORE COURSE	45	27.3
APPLIED COURSE	65	39.4
DIVERSIFIED COURSE	18	10.9
TOTAL	**165**	**100**

No. of Credits	
I YEAR	50
III TERM	29
IV TERM	29
V TERM	28
VI TERM	29
Total Credits	**165**

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CURRICULUM OUTLINE AND SCHEME OF EXAMINATIONS

PROGRAMME: Diploma in Electronics and Communication Engineering

N1–SCHEME

I TERM

Course Code	Course Name	Col No	Hours Per week			Credits	Duration of Exam in hours	Examination Marks			Minimum For pass
			Theory	Drawing	Tutorial Practical			Internal Assessment marks	External Exam Marks	Marks	
N1BE101	Communication English – I	1	4	-	-	2	3	25	75	100	40
N1BE102	Engineering Mathematics	2	7	-	-	5	3	25	75	100	40
N1BE103	Engineering Physics – I	3	5	-	-	3	3	25	75	100	40
N1BE104	Engineering Chemistry – I	4	5	-	-	3	3	25	75	100	40
N1BE201	Engineering Graphics	5	-	6	-	5	3	25	75	100	40
N1BE105	Engineering Physics - I Practical	6	-	-	2	2	3	25	75	100	50
N1BE106	Engineering Chemistry –I Practical	7	-	-	2	2	3	25	75	100	50
N1BE107	Communication Skill Practical	8	-	-	3	3	3	25	75	100	50
	Library				1						
	Total		21	6	8	25		200	600	800	-

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CURRICULUM OUTLINE AND SCHEME OF EXAMINATIONS

PROGRAMME: Diploma in Electronics and Communication Engineering

N1–SCHEME

II TERM

Course Code	Course Name	Col No	Hours Per week			Credits	Duration of Exam in hours	Examination Marks			Minimum For pass
			Theory	Drawing	Tutorial Practical			Internal Assessment marks	External Exam Marks	Marks	
N1BE109	Communication English – II	**1**	4	-	-	2	3	25	75	100	40
N1BE110	Applied Mathematics	2	6	-	-	4	3	25	75	100	40
N1BE111	Engineering Physics – II	3	4	-	-	2	3	25	75	100	40
N1BE112	Engineering Chemistry – II	4	4	-	-	2	3	25	75	100	40
N1BE202	Engineering Drawing	5	-	6	-	5	3	25	75	100	40
N1BE113	Engineering Physics – II Practical	6	-	-	2	2	3	25	75	100	50
N1BE114	Engineering Chemistry – II Practical	7	-	-	2	2	3	25	75	100	50
N1BE203	Workshop Practice	8	-	-	3	3	3	25	75	100	50
N1BE108	Computer Application Practical	9	-	-	3	3	3	25	75	100	50
	Library				1						
	Total		**18**	**6**	**11**	**25**		**225**	**675**	**900**	

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CURRICULUM OUTLINE AND SCHEME OF EXAMINATIONS

PROGRAMME: Diploma in Electronics and Communication Engineering

N1–SCHEME

III TERM

Course Code	Course Name	Col No	Hours Per week				Credits	Duration of Exam in hours	Examination Marks			Minimum For pass
			Theory	Practical	Tutorial	Total Hours			Internal Assessment marks	External Exam Marks	Marks	
N1EC204	Electronic Devices and Circuits	1	6	-	-	6	6	3	25	75	100	40
N1EC205	Electrical Circuits and Instrumentation	2	6	-	-	6	6	3	25	75	100	40
N1EC301	Programming in "C"	3	6	-	-	6	6	3	25	75	100	40
N1EC208	Electronic Devices and Circuits Practical	4	-	4	-	4	3	3	25	75	100	50
N1EC209	Electrical Circuits and Instrumentation Practical	5	-	5	-	5	3	3	25	75	100	50
N1EC309	Programming in "C" Practical	6	-	4	-	4	3	3	25	75	100	50
N1EC401	CCTV & Security Systems Practical	7	-	4	-	4	2	3	25	75	100	50
	Total		**18**	**17**	**-**	**35**	**29**		**175**	**525**	**700**	

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CURRICULUM OUTLINE AND SCHEME OF EXAMINATIONS

PROGRAMME: Diploma in Electronics and Communication Engineering

N1–SCHEME

IV TERM

Course Code	Course Name	Col No	Hours Per week				Credits	Duration of Exam in hours	Examination Marks			Minimum For pass
			Theory	Practical	Tutorial	Total Hours			Internal Assessment marks	External Exam Marks	Marks	
N1EC302	Industrial Electronics	**1**	5	-	-	5	5	3	25	75	100	40
N1EC206	Communication Engineering	2	6	-	-	6	6	3	25	75	100	40
N1EC207	Digital Electronics	3	5	-	-	5	5	3	25	75	100	40
N1EC303	Linear Integrated Circuits	4	5	-	-	5	4	3	25	75	100	40
N1EC210	Industrial Electronics and Communication Engineering Practical	5	-	5	-	5	3	3	25	75	100	50
N1EC310	Integrated Circuits Practical	6	-	5	-	5	3	3	25	75	100	50
N1EC402	Home Appliances servicing and Arduino Programming Practical	7	-	4	-	4	3	3	25	75	100	50
	Total		**21**	**14**	**-**	**35**	**29**		**175**	**525**	**700**	

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CURRICULUM OUTLINE AND SCHEME OF EXAMINATIONS

PROGRAMME: Diploma in Electronics and Communication Engineering

N1–SCHEME

V TERM

Course Code	Course Name	Col No	Hours Per week				Credits	Duration of Exam in hours	Examination Marks			Minimum For pass
			Theory	Practical	Tutorial	Total Hours			Internal Assessment marks	External Exam Marks	Marks	
N1EC304	Advanced Communication Systems	**1**	6	-	-	6	6	3	25	75	100	40
N1EC305	Microcontroller	2	6	-	-	6	6	3	25	75	100	40
N1EC306	Very Large Scale Integration	3	6	-	-	6	5	3	25	75	100	40
N1EC403	**Elective Theory - I** 1. Digital Communication	4	5	-	-	5	5	3	25	75	100	40
N1EC404	2. Mobile Communication											
N1EC405	3. Television Engineering											
N1EC311	Advanced Communication Systems Practical	5	-	4	-	4	2	3	25	75	100	50
N1EC312	Microcontroller Practical	6	-	4	-	4	2	3	25	75	100	50
N1EC313	Very Large Scale Integration Practical	7	-	4	-	4	2	3	25	75	100	50
	Total		**23**	**12**	**-**	**35**	**28**		**175**	**525**	**700**	

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CURRICULUM OUTLINE AND SCHEME OF EXAMINATIONS

PROGRAMME: Diploma in Electronics and Communication Engineering

N1–SCHEME

VI TERM

Course Code	Course Name	Col No	Hours Per week				Credits	Duration of Exam in hours	Examination Marks			Minimum For pass
			Theory	Practical	Tutorial	Total Hours			Internal Assessment marks	External Exam Marks	Marks	
N1EC307	Computer Hardware Servicing and Networking	**1**	6	-	-	6	6	3	25	75	100	40
N1EC308	Biomedical Instrumentation	2	6	-	-	6	6	3	25	75	100	40
N1EC407	**Elective Theory – II** 1. Embedded systems	3	5	-	-	5	5	3	25	75	100	40
N1EC408	2. Programmable Logic Controller											
N1CO400	3. Nano and Solar Engineering											
N1EC314	Computer Hardware Servicing and Networking Practical	4	-	5	-	5	3	3	25	75	100	50
N1EC315	PCB Design Practical	5	-	5	-	5	3	3	25	75	100	50
N1EC409	**Elective Practical – I** 1. Embedded systems Practical	6	-	4	-	4	3	3	25	75	100	50
N1EC410	2. Programmable Logic Controller Practical											
N1CO401	3. Nano and Solar Engineering Practical											
N1EC316	Project Work and Seminar	7	-	4	-	4	3	3	25	75	100	50
	Total		**17**	**18**	**-**	**35**	**29**		**175**	**525**	**700**	

INSTITUTE VISION

To be an institute of excellence in Technical Education and Training individuals focusing on the needs of the Nation and Society in tune with Technological Developments.

INSTITUTE MISSION

Our Mission is to produce Disciplined and Quality Technocrats through Academic Programme of noted excellence to serve the Society.

DEPARTMENT VISION

To be a department of excellence in Electronics and Communication Engineering and Training individuals focusing on the needs of the Nation and Society in tune with Technological Developments.

DEPARTMENT MISSION

Our Mission is to produce Disciplined and Quality Electronics and Communication Technocrats through Academic Programme of noted excellence to serve the Society.

PROGRAMME OUTCOMES (PO s)

1. **Basic and Discipline Specific Knowledge**: Apply knowledge of basic mathematics, Science and Engineering fundamentals and Engineering specialization to solve the Engineering problems.

2. **Problem Analysis**: Identify and analyse well-defined Engineering problems using codified standard methods.

3. **Design / Development of solutions**: Design solutions for well-defined technical problems and assist with the design of systems components or processes to meet specified needs.

4. **Engineering Tools, Experimentation and Testing**: Apply modern engineering tools and appropriate technique to conduct standard tests and measurements.

5. **Engineering practices for Society, Sustainability and Environment:** Apply appropriate technology in context of society, sustainability, environment and ethical practices.

6. **Project management:** Use engineering management principles individually, as a team member or a leader to manage projects and effectively communicate about well-defined engineering activities.

7. **Life-long learning:** Ability to analyse individual needs and engage in updating in the context of technological changes.

PROGRAMME SPECIFIC OUTCOMES (PSOs)

1. Apply principles to design electronic systems that perform analog and digital function.

2. Develop, validate and maintain VLSI, Embedded and CCTV based systems.

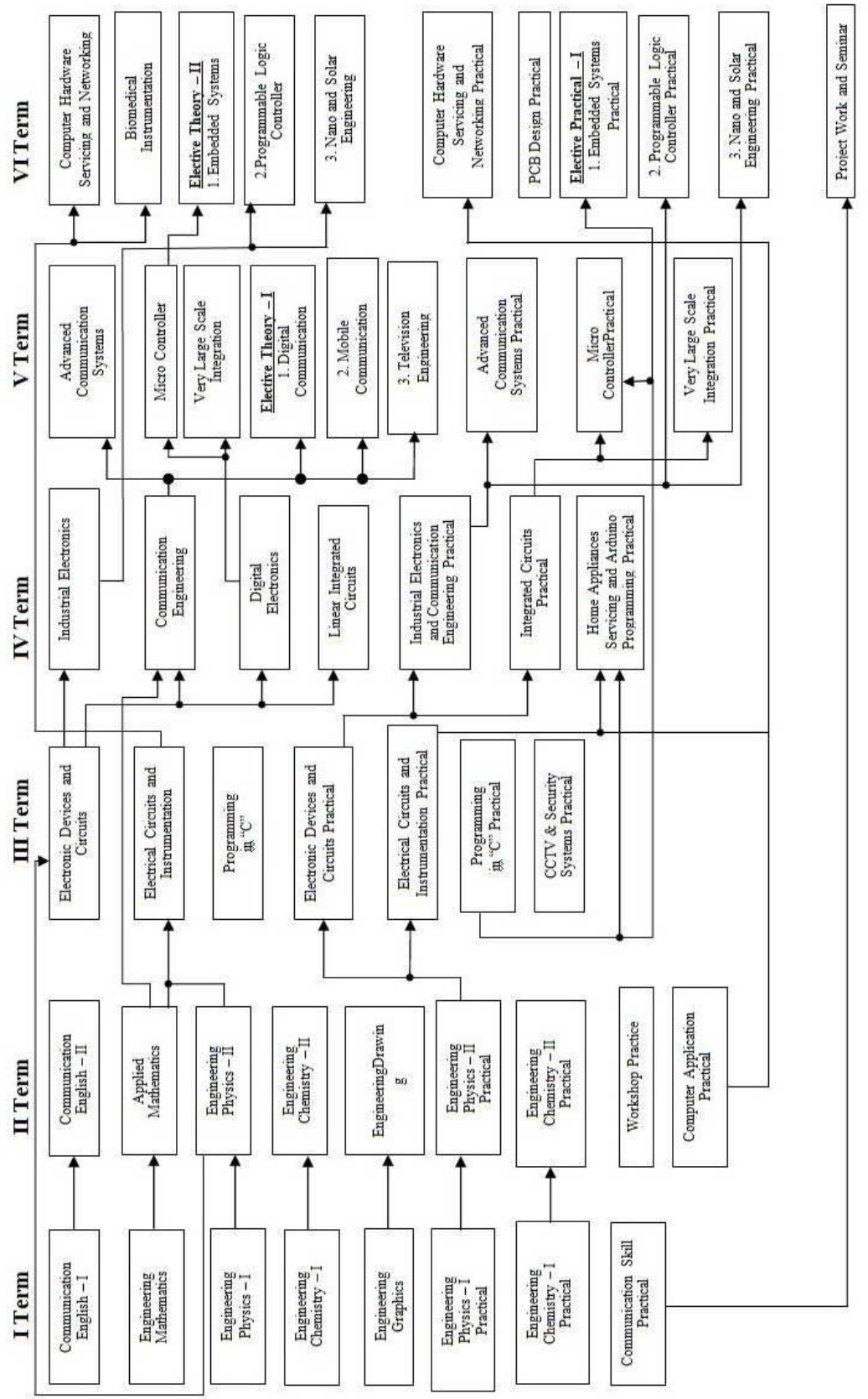
Overall Course-PO & PSO Attainment Matrix

Sl. No.	Term	Course Name	Programme Outcomes (PO's)							Programme Specific Outcomes (PSO's)	
			1	2	3	4	5	6	7	1	2
1.	III	Electronic Devices and Circuits	3	3	-	-	1	-	1	-	-
2.		Electrical Circuits and Instrumentation	3	3	-	2	-	-	2	-	-
3.		Programming in "C"	1	3	-	3	-	-	3	-	-
4.		Electronic Devices and Circuits Practical	3	3	-	2	-	-	2	-	-
5.		Electrical Circuits and Instrumentation Practical	3	3	-	2	-	1	1	-	-
6.		Programming in "C" Practical	-	3	3	3	-	-	-	-	-
7.		CCTV & Security Systems Practical	3	3	2	-	3	-	-	-	3
1.	IV	Industrial Electronics	3	2	1	-	3	-	1	-	-
2.		Communication Engineering	3	3	1	1	1	-	1	-	-
3.		Digital Electronics	3	3	3	-	1	-	-	2	-
4.		Linear Integrated Circuits	3	3	1	1	1	-	3	3	1
5.		Industrial Electronics and Communication Engineering Practical	3	3	2	2	-	-	1	-	-
6.		Integrated Circuits Practical	3	3	3	-	-	-	-	3	-
7.		Home Appliances servicing and Arduino Programming Practical	3	2	1	1	3	-	-	-	-

Sl. No.	Term	Course Name	Programme Outcomes (PO's)							Programme Specific Outcomes (PSO's)	
			1	2	3	4	5	6	7	1	2
1.	V	Advanced Communication Systems	1	3	-	1	3	-	2	-	-
2.		Microcontroller	3	3	2	-	1	-	1	-	-
3.		Very Large Scale Integration	3	3	-	3	2	-	3	1	3
4.		**Elective Theory – I** 1. Digital Communication	3	1	3	-	1	-	1	3	-
4.		2. Mobile Communication	2	-	3	-	3	-	-	-	-
4.		3. Television Engineering	3	1	-	1	3	-	1	2	2
5.		Advanced Communication Systems Practical	3	3	-	3	-	-	-	-	-
6.		Microcontroller Practical	3	3	2	2	-	-	-	-	-
7.		Very Large Scale Integration Practical	-	3	3	3	2	-	-	-	3
1.	VI	Computer Hardware Servicing and Networking	1	3	3	-	3	-	-	-	-
2.		Biomedical Instrumentation	3	3	-	-	3	-	1	-	-
3.		**Elective Theory – II** 1. Embedded systems	3	2	2	1	-	-	1	1	3
3.		2. Programmable Logic Controller	1	3	1	1	3	-	1	-	-
3.		3. Nano and Solar Engineering	3	2	3	3	2	-	1	-	3
4.		Computer Hardware Servicing and Networking Practical	3	3	-	3	1	-	-	-	-
5.		PCB Design Practical	1	3	3	3	-	-	-	-	-
6.		**Elective Practical – I** 1. Embedded systems Practical	1	3	3	1	1	-	1	1	3
6.		2. Programmable Logic Controller Practical	1	1	1	1	3	3	3	-	-
6.		3. Nano and Solar Engineering Practical	3	3	-	3	-	-	-	-	3
7.		Project Work and Seminar	1	2	3	1	2	3	3	-	-

Course Pre-requisites for the curriculum of Diploma in ECE

(N1 Scheme)



VIRUDHUNAGAR S.VELLAICHAMY NADAR POLYTECHNIC COLLEGE (AUTONOMOUS)

(Affiliated to Directorate of Technical Education, Chennai-25)

VIRUDHUNAGAR – 626 001

N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering
Course code : N1EC204
Term : III
Course Name : ELECTRONIC DEVICES AND CIRCUITS

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
Electronic Devices and Circuits	Hours / Week	Hours / Term	Marks			Duration
	6	90	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Hours
1	Semiconductor and Diodes	18
2	Bipolar Junction Transistor	18
3	Transistor oscillators, FET and UJT	18
4	SCR,DIAC,TRIAC and MOSFET	18
5	Opto Electronic Devices and Wave shaping Circuits	18
	Total	90

Course Outcomes:

On successful completion of the course, the student will be able to:

C204.1	Know about the semiconductor and diodes.
C204.2	Gain knowledge about the Bipolar Junction Transistors.
C204.3	Understand the working of transistor oscillators, FET and UJT.
C204.4	Elucidate the thyristor family.
C204.5	Familiarize the Opto electronic devices and Wave shaping circuits.

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Teaching Hrs
C204.1	Know about the semiconductor and diodes.	**R/U/A**	1,2	18
C204.2	Gain knowledge about the Bipolar Junction Transistors.	**R/U/A**	1,2	18
C204.3	Understand the working of transistor oscillators, FET and UJT.	**R/U/A**	1,2	18
C204.4	Elucidate the thyristor family.	**R/U/A**	1,2,5	18
C204.5	Familiarize the Opto electronic devices and Wave shaping circuits.	**R/U/A**	1,2,5,7	18
		Total sessions		90

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	Semiconductor and Diodes	18	25	***2***	***18***	***5***	*17.86*
II	Bipolar Junction Transistor	18	25	***2***	***18***	***5***	*17.86*
III	Transistor oscillators, FET and UJT	18	25	***2***	***18***	***5***	*17.86*
IV	SCR,DIAC,TRIAC and MOSFET	18	25	***2***	***18***	***5***	*17.86*
V	Opto Electronic Devices and Wave shaping Circuits	18	25	***2***	***18***	***5***	*17.86*
I to V			15	***6***	***9***	***0***	*10.70*
	Total		**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
Electronic Devices and Circuits	**3**	**3**	**-**	**-**	**1**	**-**	**1**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**SEMICONDUCTOR AND DIODES:** **SEMICONDUCTOR:** Definition – Classification - Intrinsic and Extrinsic semiconductor, N type & P type – Drift Current & Diffusion current. Diodes - PN junction diode - Forward and Reverse bias Characteristics – Specification – Zener diode-Construction & working principle - Characteristics – Cut in voltage and breakdown voltage - Zener break down-Avalanche break down- Zener diode as a voltage regulator – Applications - Specification. **RECTIFIER** – Introduction – Classification of Rectifiers – Half Wave Rectifier – Full Wave Rectifier – Bridge Rectifier – Efficiency – Ripple factor (definition and values only) – Applications – Filters – C, LC and PI Filters (Concept only).	18
II	**BIPOLAR JUNCTION TRANSISTOR:** **TRANSISTOR:** NPN and PNP transistor operation – CB, CE, CC Configurations – Characteristics – cut off and saturation – Comparison between three configurations in terms of input impedance, output impedance, current gain, voltage gain- Transistor as an amplifier - Transistor as a switch.(simple problems using α & β) - Biasing – Fixed biasing – Voltage divider Biasing. RC coupled amplifier – Operation & Frequency response - Emitter follower and its application – Negative feedback – Basic concept, effect of negative feedback, Types of Negative feedback connections.	18
III	**TRANSISTOR OSCILLATORS, FET AND UJT:** **TRANSISTOR OSCILLATORS :** Classifications – Condition for oscillations (Barkhausen criterion) – General form of LC oscillator – Hartley Oscillator – Colpitts Oscillator – RC Phase shift oscillator, Crystal oscillator. **FIELD EFFECT TRANSISTOR** : Construction – Working principle of FET – Difference between FET and BJT – Characteristics of FET – Applications – FET amplifier (Common source amplifier). **UNI JUNCTION TRANSISTOR** : Construction – Equivalent circuit – Operation – Characteristics – UJT as a relaxation oscillator.	18

IV	**SCR, DIAC, TRIAC AND MOSFET :** **SCR** – Introduction – Working – Two transistor analogy of SCR – VI characteristics – Forward break over voltage – holding current – Latching current – Reverse break down voltage (Definition) – SCR as a Switch, Controlled rectifier. **TRIAC** – Basic working principle – Characteristics. **DIAC** – Construction – Working – Characteristics – DIAC as bi-directional switch – Speed control of fan using DIAC and TRIAC. **MOSFET** – Construction – Characteristics – MOSFET as a Switch.	18
V	**OPTO-ELECTRONIC DEVICES AND WAVE SHAPING CIRCUITS:** **OPTO-ELECTRONIC DEVICES:** LDR, LED, 7 segment LED, LCD, Opto coupler, Opto interrupter – Infrared transmitter and Receiver – Laser diode (simple treatment) – Solar cell – Avalanche Photodiode – Photo transistor, Organic LED. **WAVE SHAPING CIRCUITS:** Clipper, clamper circuits using diode – Voltage doubler, Astable, Monostable and Bistable operations using Transistor-Schmitt Trigger.	18

Text Book:

1. Electronics Devices & Circuits by Salivahanan, N. Suresh Kumar, A. Vallavaraj, Tata McGraw Publication.
2. Principle of Electronics by V.K. Mehta, S. Chand & Company ltd.

Reference Book:

1. Electronic Devices and Circuits by Boylestead, Tata McGraw Publication.
2. Electronic Devices & Circuits by A.P. Godse & U.A. Bakshi, Technical Publications.
3. Fundamentals of Electrical Engineering and Electronics by B.L. Theraja, S.Chand & company Pvt.Ltd.
4. Electronics principles by Malvino, Tata McGraw Publication.
5. Electronics Devices & Circuits by Allen Mottershed, Tata McGraw Hill Publication.
6. Electronics Devices & Circuits by Jacob Millman and Halkias, Tata McGraw Hill publication.
7. Optical Fiber Communication by Gerd Keiser.

MODEL QUESTION PAPER – I

Term : III Time : 3hrs

Programme : Diploma in Electronics and Communication Engineering Max. Marks :75

Course : Electronic Devices and Circuits Course Code : N1EC204

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Give the classification of semi conductor.
2. Draw the symbol of NPN and PNP transistor. Mark the terminals.
3. Draw the equivalent circuit of UJT.
4. Draw the symbol of a TRIAC. Name its terminals.
5. State the classification of multivibrators.
6. Classify negative feedback connection?
7. What is LDR ?
8. State Barkhausen Criteria.

PART – B

9. Draw a zener diode voltage regulator circuit.
10. Compare CE, CB, CC transistor configurations.
11. Draw a crystal oscillator circuit.
12. Compare SCR and Transistor.
13. Briefly explain about Solar Cell .
14. Draw the symbol of n-channel MOSFET for depletion and enhancement modes.
15. Explain a simple positive clipper.
16. Classify transistor biasing circuits.

[Turn over …..

PART – C

17. (a) Explain the working of PN junction diode with necessary diagrams.

(Or)

(b) Explain the working of a bridge rectifier with a neat circuit diagram. Draw its input and output waveform.

18. (a) Explain the output characteristics of a transistor in common emitter configuration

(Or)

(b) Explain the construction and operation of NPN transistor with neat diagram.

19. (a) Explain the working of a RC phase shift oscillator with a neat sketch and write the equation for frequency of oscillation for a RC phase shift oscillator.

(Or)

(b) Explain the construction and working of an n- channel FET with necessary diagrams. Draw the characteristics of a FET.

20. (a) Explain the working of SCR and draw the characteristics curve.

(Or)

(b) Explain the working and the VI characteristics of TRIAC .

21. (a) Explain about: (i) Opto coupler (ii) Photo transistor

(Or)

(b) Explain the working of an astable multivibrator with circuit diagram and waveforms .

MODEL QUESTION PAPER - II

Term : III Time : 3hrs
Programme : Diploma in Electronics and Communication Engineering Max. Marks :75
Course : Electronic Devices and Circuits Course Code : N1EC204

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.
(2) Answer division (a) or division (b) of each question in PART – C.
(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define intrinsic semiconductor.
2. Give the applications of emitter follower.
3. State the conditions for oscillations?
4. Draw the symbol of DIAC. Name its terminals.
5. What is bistable multivibrators.
6. What are the effects of negative feedback connection?
7. Draw the symbol of n-channel and p-channel FET?
8. Define rectifier?

PART – B

9. Compare zener and avalanche breakdown.
10. Explain how a transistor works as a switch
11. Draw the circuit of RC phase shift oscillator.
12. Explain the working of DIAC as a bidirectional switch .
13. Briefly explain about voltage doubler .
14. Draw the symbol of n-channel MOSFET for depletion and enhancement modes.
15. Explain a simple negative clipper .
16. Compare CE, CB, CC transistor configurations.

[Turn over …..

PART – C

17. (a) Explain the working and Characteristics of Zener diode with necessary diagrams.

(Or)

(b) Explain the working of a center tap full wave rectifier with a neat circuit diagram. Draw input and output waveform.

18. (a) Explain the output characteristics of a transistor in common base configuration .

(Or)

(b) Explain the construction and operation of PNP transistor with neat diagram.

19. (a) Explain the working of a Hartley oscillator with a neat sketch and write the equation for frequency of oscillation for Hartley oscillator.

(Or)

(b) Explain the construction and working of UJT with necessary diagrams. Draw the characteristics of a UJT.

20. (a) Explain the working of TRIAC and draw its characteristics.

(Or)

(b) Explain the working of n-channel enhancement MOSFET . Draw its drain characteristics.

21. (a) Explain about: (i) Solar Cell (ii) Positive Clamper.

(Or)

(b) Explain the working of an Monostable multivibrator with circuit diagram and waveforms.

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N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC205

Term : III

Course Name : ELECTRICAL CIRCUITS AND INSTRUMENTATION

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
ELECTRICAL CIRCUITS AND INSTRUMENTATION	Hours / Week	Hours / Term	Marks			Duration
	6	90	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Hours
I	D.C. CIRCUITS AND THEOREMS	18
II	A.C. CIRCUITS AND RESONANCE	18
III	TRANSFORMERS AND MACHINES	18
IV	MEASURING INSTRUMENTS AND CRO	18
V	TRANSDUCERS ,SENSORS & TEST INSTRUMENTS	18
	Total	90

Course Outcomes:

On successful completion of the course, the student will be able to:

C205.1	Familiarize different DC circuits and theorems.
C205.2	Understand the AC circuits and resonance.
C205.3	Understand the working of various electric machines.
C205.4	Understand the working principles of different measuring instruments and CRO.
C205.5	Familiarize with digital multi meter, recorders, sensors and transducers.

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Teaching Hrs
C205.1	Familiarize different DC circuits and theorems.	**R/U/A**	1,2,4	18
C205.2	Understand the AC circuits and resonance.	**R/U/A**	1,2,4	18
C205.3	Understand the working of various electric machines.	**R/U/A**	1,2,4	18
C205.4	Understand the working principles of different measuring instruments and CRO.	**R/U/A**	1,2,4,7	18
C205.5	Familiarize with digital multi meter, recorders, sensors and transducers.	**R/U/A**	1,2,4,7	18
		Total sessions		90

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	D.C. CIRCUITS AND THEOREMS	18	25	***2***	***18***	***5***	*17.86*
II	A.C. CIRCUITS AND RESONANCE	18	25	***2***	***18***	***5***	*17.86*
III	TRANSFORMERS AND MACHINES	18	25	***2***	***18***	***5***	*17.86*
IV	MEASURING INSTRUMENTS AND CRO	18	25	***2***	***18***	***5***	*17.86*
V	TRANSDUCERS, SENSORS & TEST INSTRUMENTS	18	25	***2***	***18***	***5***	*17.86*
I to V			15	***6***	***9***	***0***	*10.70*
	Total	90	**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
Electrical Circuits And Instrumentation	**3**	**3**	**-**	**2**	**-**	**-**	**2**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**D.C. CIRCUITS AND THEOREMS** **D.C. CIRCUITS:** Definition and unit for voltage, current, power, resistance, conductance, resistivity – ohm's law – only simple problems in ohm's law- Kirchoff's current law and voltage law. **THEOREMS**: Series circuits – parallel circuits – series parallel circuits – Thevenin's, Norton's, super position and maximum power transfer theorem – Statement and explanation (simple problems – two sources with four resistors)	18
II	**A.C. CIRCUITS AND RESONANCE** **A.C. CIRCUITS:** AC through single pure resistance, pure inductance, pure capacitance – voltage and current relationship – and (to mention only) the equation for power and power factor in each case (only simple problems). Definition for impedance, reactance, admittance, conductance, phase angle, power factor and power. AC circuits – Derivation only for impedance, power and power factor in Series R-L, R-C, R-L-C circuits. Analysis of Parallel R-L circuit, R-C circuit, R-L-C circuit (Qualitative treatment only) **RESONANCE:** Resonance – series resonance – parallel resonance – condition for resonance – resonant frequency – Q factor – resonance curve – bandwidth (only simple problems).	18
III	**TRANSFORMERS AND MACHINES** **TRANSFORMERS:** Transformer – Ideal transformer – construction – working principle – EMF equation – Losses in transformer – core loss, copper loss – Efficiency – Regulation – OC, SC test on transformer – List of applications (qualitative treatment only) **MACHINES :** D.C Machines – DC Generator – Working principle – Types – Applications – DC motor – working principle – types –applications (qualitative treatment only) Single phase Induction motor – Types – construction & principle of operation of capacitor start induction motor – Applications – stepper motor – working principle – uses (qualitative treatment only). Universal Motor (qualitative treatment only). Difference between single phase and three phase supply	18

IV	**MEASURING INSTRUMENTS AND CRO** **MEASURING INSTRUMENTS:** Indicating instruments – Types of Indicating instruments (MI, MC), Comparison – Basic forces for indicating instruments – construction and operation of permanent magnet moving coil Instrument – Advantages – Disadvantages of PMMC – Shunts and Multipliers – DC ammeter – DC volt meter – volt meter sensitivity. Bridges – Types – Wheat stone bridge – applications – Universal impedance bridge arrangements to measure R,L,C. **CRO :** CRO – Block diagram and principle of operation of CRO – operation of CRT – Electrostatic focusing – Electrostatic deflection (no derivation) – Block diagram of vertical deflection system – Applications of CRO – Types of CRO – Block diagram and operation of dual trace CRO – dual beam CRO – comparison between dual trace and dual beam CRO – Digital storage oscilloscope – Block diagram – advantages. advantage. Block diagram-working principle of Function Generator.	18
V	**TRANSDUCERS, SENSORS & TEST INSTRUMENTS** **TRANSDUCERS** Transducers – classification of transducer – Strain gauge – Types – uses. Construction, operation and applications of photo electric transducer, LVDT ,RVDT and Load cell. Principle of working of thermocouple – Temperature measurement using thermocouple – list of applications – Principle of working of Thermistor – Temperature measurement using thermistors – Types (NTC, PTC) – List of applications . **SENSORS** IR range sensor – IR proximity sensor – Ultrasonic range sensor – Touch sensor. **TEST INSTRUMENTS:** Digital voltmeter – Types (to list only) – Basic block diagram of DVM – Block diagram of Digital multi meter – Advantages over analog instruments – Block diagram of Digital frequency counter – Simple PC based Data Acquisition system – Block diagram.	18

Text Book :

1. A text book of Electrical Technology by B.L. Theraja, Publication Division of Nirja constructions and development co. (P) Ltd., - 1994.
2. Electrical and Electronic- Measurements and Instrumentation by A.K.Sawheney- Dhanpatrai and Sons -1993.

Reference Book:

1. Electric circuit theory by Dr. M. Arumugam, N. Premkumaran.
2. Modern Electronic Instrumentation and Measurement Techniques by Albert D.Hel frick and Willam David cooper- Prentice Hall of India Pvt. Ltd., 1996.

MODEL QUESTION PAPER – I

Term : III Time : 3 Hrs

Programme :Diploma in Electronics and communication Engineering Max. Marks : 75

Course : Electrical Circuits and Instrumentation Course Code : N1EC205

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define Ohms law.
2. What is the equivalent resistance of three resistances R1, R2, R3 connected in parallel?
3. What is meant by resonance?
4. What are the applications of transformer?
5. What are the types of DC generators?
6. What are the basic forces for indicating instruments?
7. What is meant by NTC, PTC?
8. What is use of DAS?

PART – B

9. Define voltage, current, resistance.
10. Compare series and parallel resonance.
11. Draw the resonance curve and define bandwidth.
12. What are the losses in transformer?
13. List the applications of different DC Motors.
14. Compare dual beam and dual trace CRO.
15. Write the advantages of DSO.
16. Explain the Working Principle of thermocouple.

[Turn over …..

PART – C

17. a) State and explain the Norton's theorem with Diagram.

(or)

b) Derive the condition for maximum power transfer in a circuit.

18. a) Derive the expression for resonance frequency and Q factor of a series resonance circuit.

(or)

b) Derive the expression for impedance of an RLC series circuit.

19. a) Explain the working of transformer.

(or)

b) How a stepper motor works? Explain with Diagram.

20. a) Explain the working of Basic CRO with diagram.

(or)

b) Draw and explain the working of PMMC instrument.

21. a) Explain the construction and working of LVDT.

(or)

b) Draw the simple PC based Data acquisition system and give its advantages.

MODEL QUESTION PAPER – II

Term : III Time : 3 Hrs

Programme :Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : Electrical Circuits and Instrumentation Course Code : N1EC205

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.
(2) Answer division (a) or division (b) of each question in PART – C.
(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define Resistance, conductance.
2. What is the total resistance when R1, R2, R3 are connected in series?
3. What is the condition for resonance in series resonance circuit?
4. What are the losses in Transformer?
5. What is Calibration?
6. What are the applications of CRO?
7. List Different type of sensor.
8. What are the types of Digital volt meter?

PART – B

9. State Norton's theorem and give formula for IL.
10. Define phase angle, power factor in AC circuit.
11. What is the difference between single phase and three phase supply?
12. What is the difference between dual beam and dual trace CRO?
13. What are the basic forces of Indicating Instruments?
14. Give short notes on shunt and multipliers.
15. What is transducer and give their classification?
16. What are the advantages of digital meters over analog meters?

[Turn over …..

PART – C

17. a) State and explain super position theorem with diagram.

(Or)

b) State explain Thevenin's theorem with diagram.

18. a) Derive the expression for Z, I, Power, Power factor for a RL circuit with diagram.

(Or)

b) a) Derive the resonance frequency for sensors Ac circuit.
b) Compare series and parallel resonance circuit.

19. a) Explain OC.SC test on transformer.

(Or)

b) Explain single phase induction motor working with diagram.

20. a) Explain the working of universal bridge with diagram.

(Or)

b) Explain the working of function generator with diagram.

21. a) Explain the characteristics of different temperature sensor.

(Or)

b) Explain with diagram working of Digital multimeter.

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N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC301

Term : III

Course Name : PROGRAMMING IN "C"

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
PROGRAMMING IN "C"	Hours / Week	Hours / Term	Marks			Duration
	6	90	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Hours
1.	PROGRAM DEVELOPMENT AND INTRODUCTION TO C	17
2.	C OPERATORS AND DECISION MAKING	18
3.	ARRAYS, STRINGS AND FUNCTIONS	19
4.	STRUCTURES, UNIONS, DYNAMIC MEMORY AND FILE MANAGEMENT	18
5.	POINTERS AND "C" PROGRAMMING	18
	Total	90

Course Outcomes:

On successful completion of the course, the student will be able to:

C301.1	Develop algorithm and flow-chart to solve a problem and familiarize C tokens.
C301.2	Familiarize C operators, Branching and Looping statements.
C301.3	Use arrays, strings and functions in simple programs.
C301.4	Employ structures, unions and dynamic memory allocation and file handling.
C301.5	Understand pointer concept and develop simple C programs.

Course Outcome linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Teaching Hrs.
C301.1	Develop algorithm and flow-chart to solve a problem and familiarize C tokens.	**R/U/A**	1,2,4	17
C301.2	Familiarize C operators, Branching and Looping statements.	**R/U/A**	2,4	18
C301.3	Use arrays, strings and functions in simple programs.	**R/U/A**	2,4,7	19
C301.4	Employ structures, unions and dynamic memory allocation and file handling.	**R/U/A**	2,4,7	18
C301.5	Understand pointer concept and develop simple C programs.	**R/U/A**	2,4,7	18
		Total sessions		90

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	PROGRAM DEVELOPMENT AND INTRODUCTION TO C	17	25	**2**	**18**	**5**	17.86
II	C OPERATORS AND DECISION MAKING	18	25	**2**	**18**	**5**	17.86
III	ARRAYS ,STRINGS AND FUNCTIONS	19	25	**2**	**18**	**5**	17.86
IV	STRUCTURES,UNIONS, DYNAMIC MEMORY AND FILE MANAGEMENT	18	25	**2**	**18**	**5**	17.86
V	POINTERS AND "C" PROGRAMMING	18	25	**2**	**18**	**5**	17.86
I to V *			15	**6**	**9**	**0**	10.70
	Total	90	**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
PROGRAMMING IN "C"	**1**	**3**	**--**	**3**	**--**	**--**	**3**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

UNIT	NAME OF THE TOPIC	HOURS
I	**PROGRAM DEVELOPMENT AND INTRODUCTION TO C :** **1.1 Program, Algorithm & flow chart:** Program development cycle-Programming language levels and features. Algorithm – Properties & classification of Algorithm, flow chart – symbols, importance and advantage of flow chart. **1.2 Introduction to C:** History of C – features of C- structure of C program – Compile, link and run a program. Diagrammatic representation of program execution process. **1.3 Variables, Constants & Data types:** C character set-Tokens-Constants- Key words – Identifiers and Variables – Data types and storage – Data type Qualifiers – Declaration of Variables – Assigning values to variables- Declaring variables as constants-Declaring variables as volatile- Overflow & under flow of data.	17
II	**C OPERATORS AND DECISION MAKING:** **2.1 C operators:** Arithmetic, Logical, Assignment, Relational, Increment and Decrement, Conditional, Bitwise, Special – Operator precedence and Associativity – C expressions – Arithmetic expressions – Evaluation of expressions- Type cast operator. **2.2. I/O statements:** Formatted input, formatted output, Unformatted I/O statements. **2.3 Branching:-** Introduction – Simple if statement – if –else – else-if ladder , nested if-else – Switch statement – go statement. **2.4 Looping statements:-** While, do-while statements, for loop, break & continue statement.	18
III	**ARRAYS, STRINGS AND FUNCTIONS:** **3.1 Arrays:** Declaration and initialization of One dimensional, Two dimensional and Character arrays – Accessing array elements – Simple Programs using arrays. **3.2 Strings :** Declaration and initialization of string variables, Reading String, Writing Strings – String handling functions. (strlen(),strcat(),strcmp()) – Simple String manipulation programs. **3.3 Built –in functions:** Math functions – Console I/O functions - Standard I/O functions – Character Oriented functions. **3.4 User defined functions:-** Defining functions & Needs-Scope and Life time of Variables- Function call, return values-Storage Classes - Category of function – Recursion.	19

IV	**STRUCTURES, UNIONS, DYNAMIC MEMORY AND FILE MANAGEMENT:** **4.1 Structures and Unions:** Structure – Definition, initialization, arrays of structures, Arrays within structures, structures within structures, Structures and functions – Unions – Structure of Union – Difference between Union and structure. **4.2 Dynamic Memory Management:-** introduction – dynamic memory allocation – allocating a block memory (MALLOC) – allocating multiple blocks of memory (CALLOC) – releasing the used space(free) - altering the size of a block (REALLOC). **4.3 File Management:** Introduction – Opening a file - Closing a file - Input/output operations on files - Program to read data from the keyboard, write it to a file and display it on the screen.	18
V	**POINTERS AND "C" PROGRAMMING:** **5.1 Pointers:** Introduction - Definition - Syntax - Accessing the address of a variable, Declaring and initializing pointers, Accessing a variable through its pointer - Advantages of pointers. **5.2** Program to find Sum of Series using "while" loop- Program to find Factorial of N numbers using functions- Program to swap the values of two variables. **5.3** Program to implement Ohms Law- Program to find Resonant Frequency of RLC Circuit- Program to find equivalent resistance of three resistances connected in series and parallel-Program to print the address of the variable using Pointer - Program to Concatenate two strings using string functions. **5.4** Program to draw the symbol of NPN transistor using Graphics- Program to draw the symbol of diode using Graphics.	18

Text Book:

1. Programming in ANSI C 7E by Prof. E. BALAGURUSAMY, the TATA McGRAW – HILL publications.

Reference Book:

S.No.	Title	Author	Publisher
1.	Programming and Problem solving using C	ISRD Group, Lucknow	Tata Mc-GrawHill, New Delhi
2.	Let us C	Yeswanth Kanetkar	BPB Publications
3.	A Text Book on C	E.Karthikeyan	PHI Private Limited, New Delhi
4.	Programming in C	D.Ravichandran	NewAge International Publishers
5.	Computer Concepts And Programming in C	Dr.S.S.Khandare	S.Chand & Company Ltd. New Delhi
6.	Complete Knowledge in C	Sukhendu Dey, Debobrata Dutta	Narosa Publishing House, NewDelhi
7.	Practical C Programming	Steve Oualline O'Reilly, Shroff Publishers	Eleventh Indian ReprintOct2010

MODEL QUESTION PAPER - I

Term	:	III	Time	: 3 Hrs
Programme	:	Diploma in Electronics and Communication Engineering	Max. Marks	: 75
Course	:	Programming in "C"	Code	: N1EC301

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define Algorithm.
2. What is an identifier?
3. Write down the syntax of simple if statement.
4. What do you mean by call by reference?
5. What are built in functions?
6. What is the use of struct keyword?
7. Define pointer.
8. List any two looping statements.

PART – B

9. Explain while loop with example.
10. What is string? Write a program to read a string.
11. Explain recursion with simple example.
12. How will you allocate block of memory during run time?
13. How will you declare and initialize a pointer variable?
14. Compare structures and unions.
15. What is the use of continue statement?
16. What is a flow chart? Draw the symbols used in flow chart.

[Turn over …..

PART – C

17. (a) Discuss the Program development cycle in detail.

(Or)

(b) Explain in detail about the structure of a C program with an example.

18. (a) Explain the various operators in C with one example for each operator.

(Or)

(b) Explain for loop with syntax and example.

19. (a) Explain String handling functions with example.

(Or)

(b) Explain Math functions.

20. (a) Explain Structures with simple program.

(Or)

(b) Write a program to demonstrate realloc() and free() functions.

21. (a) Write a C program to implement Ohm's Law.

(Or)

(b) Write a C Program to draw the symbol of NPN transistor using graphics.

MODEL QUESTION PAPER - II

Term	:	III	Time	: 3 Hrs
Programme	:	Diploma in Electronics and Communication Engineering	Max. Marks	: 75
Course	:	Programming in "C"	Code	: N1EC301

PART – A

1. What is algorithm of a programming language?
2. What are the levels of programming languages?
3. What are the logical operators used in C language?
4. Define loop operation.
5. What is user defined are built in function?
6. What is array?
7. What is union? Give one example.
8. How to access pointer variable in C?

PART – B

9. What are key words? Give few examples.
10. Write a program to find whether the student is "PASS" using simple if statement.
11. What is the role of branching instruction in C programming?
12. Define break and continue statement.
13. What is the role of string compare function?
14. What is the application of built in function?
15. What is dynamic memory allocation? Give one example.
16. Define pointer to the function with example.

[Turn over …..

PART – C

17. (a) What are the data types used in C programming? Explain with example.

(Or)

(b) Explain in detail about the structure of a C program with an example.

18. (a) Explain the formatted and unformatted I/O statements with an example.

(Or)

(b) What are the looping statements used in C programming? Illustrate with an example.

19. (a) Explain String handling functions with example.

(Or)

(b) Explain recursive function with an example.

20. (a) Compare structures and union with example.

(Or)

(b) What is the file management systems used in C language?

21. (a) Write a C program to find resonant frequency of RLC series circuit.

(Or)

(b) Write a C Program to concatenate two strings using string function.

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(Affiliated to Directorate of Technical Education, Chennai-25)

VIRUDHUNAGAR – 626 001

N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC208

Term : III

Course Name : Electronic Devices and Circuits Practical

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
Electronic Devices and Circuits Practical	Hours / Week	Hours / Term	Marks			Duration
	4	60	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C208.1	Understand various semiconductor device characteristics.
C208.2	Understand the applications of diodes
C208.3	Understand the waveform of multivibrator and oscillator
C208.4	Study different opto electronic devices

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		Linked Expts.	CL	Linked PO	Teaching Hrs
C208.1	Understand various semiconductor device characteristics	**1,2,5,6,8, 9,10,11**	**R,U,A**	1,2	**30**
C208.2	Understand the applications of diodes	**3,4,12,13**	**R,U,A**	1,2,4	**15**
C208.3	Understand the waveform of multivibrator and oscillator	**7,16**	**R,U,A**	1,2,4,7	**7**
C208.4	Study different opto electronic devices	**14,15**	**R,U,A**	1,2,7	**8**
Total sessions					60

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
ELECTRONIC DEVICES AND CIRCUITS PRACTICAL	**3**	**3**	**-**	**2**	**-**	**-**	**2**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

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- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
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LIST OF EXERCISES

1. Construct and plot the VI characteristics of PN junction diode and find the cut-in voltage.
2. Construct and plot the VI characteristics of Zener diode and find the break down voltage.
3. a. Simulate and Construct the Half wave rectifier with and without filters and draw the input and output waveform.
   b. Simulate and Construct the Full wave rectifier with and without filters and draw the input and output waveform.
4. Simulate and Construct and draw the input and output waveform of Bridge rectifier with and without filters.
5. Construct and draw the Input and output characteristics of CE Transistor configuration and find its input & output resistance.
6. Construct and draw the frequency response of RC coupled amplifier and determine the 3-db bandwidth.
7. Construct and draw the output waveform for RC phase shift oscillator. Find its frequency of oscillation.
8. Construct and plot the drain characteristics of JFET and find its pinch off voltage.
9. Construct and plot UJT characteristics and find its Ip and Vv.
10. Construct and plot the DIAC characteristics.
11. Construct and study the working of SCR and TRIAC.
12. Construct diode clippers and draw the output waveforms.
13. Construct diode clampers and draw the output waveforms.
14. Construct and draw LDR characteristics.
15. Construct and plot the VI characteristics of Photo transistor.
16. Simulate and construct Astable multivibrator using transistors and draw the output waveform.

Content Beyond Syllabus.

*** Simulate the VI characteristics of PN Junction Diode.**

LIST OF EQUIPMENTS

Sl. No.	Name of the Equipments	Required Nos.
1	Power supply with various o/p voltages	10
2	Electronic components	3 on each type
3.	Meters, multimeters	10 on each type
4.	Resistors, rheostats	5 on each type
5.	Connecting wires	100 mts

END EXAMINATION

Scheme of valuation in TEE		
1.	CIRCUIT DIAGRAM	20
2.	CONNECTION	25
3.	EXECUTION & HANDLING OF EQUIPMENT	15
4.	OUTPUT / RESULT	10
5.	VIVA – VOCE	05
	Total	**75**

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N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC209

Term : III

Course Name : ELECTRICAL CIRCUITS AND INSTRUMENTATION PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
ELECTRICAL CIRCUITS AND INSTRUMENTATION PRACTICAL	Hours / Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C209.1	Prove the fundamental laws of Electrical theorem
C209.2	Handle the CRO effectively.
C209.3	Handle Multimeter effectively.
C209.4	Study the characteristics of various transducers.

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		Linked Expts.	CL	Linked PO	Teaching Hrs
C209.1	Prove the fundamental laws of Electrical theorem	**1, 2, 3, 4, 5, 6**	**R,U,A**	1,2	**20**
C209.2	Handle the CRO effectively	**11, 12, 14**	**R,U,A**	1,2,4	**15**
C209.3	Handle Multimeter effectively.	**7, 8, 9, 10**	**R,U,A**	1,2,4	**20**
C209.4	Study the characteristics of various transducers	**13, 14, 15, 16**	**R,U,A**	1,2,6,7	**20**
			Total sessions		**75**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
ELECTRICAL CIRCUITS AND INSTRUMENTATION PRACTICAL	**3**	**3**	**-**	**2**	**-**	**1**	**1**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

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LIST OF EXERCISES

1. Verify ohm's law.
2. Verify Kirchoff's voltage and current law.
3. Verify super position theorem.
4. Verify Thevenin's Theorem.
5. Verify Norton's Theorem.
6. Verify maximum power transfer Theorem.
7. Calibrate the given ammeter and voltmeter.
8. Extend the range of given voltmeter.
9. Extend the range of given ammeter.
10. Study of Wheatstone bridge.
11. Measure the DC voltage, AC voltage, Frequency using CRO.
12. Measure the amplitude and frequency of two signals using dual trace CRO.
13. Study the characteristics of LVDT.
14. Measure the frequency and phase angle using CRO by Lissajous figure.
15. Study the characteristics of a thermistor, thermo couple and RTD.
16. Study the characteristics of a load cell.

LIST OF EQUIPMENTS

Sl. No.	Name of the Equipments	Required Nos.
1	Power Supply (various output voltages)	6
2	Resistors, Rheostats	20 in each type
3	Ammeter, Voltmeter, Multimeter	10 in each type
4	Instruments (Sensors with kits)	2 in each type
5	Connecting wire	100 mts

Detailed Allocation of Marks for External Assessment

Scheme of valuation in TEE		
1.	CIRCUIT DIAGRAM	30
2.	CONNECTION	20
3.	EXECUTION & HANDLING OF EQUIPMENT	10
4.	OUTPUT / RESULT	10
5.	VIVA-VOCE	05
	Total	**75**

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N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC309

Term : III

Course Name : PROGRAMMING IN "C" PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
PROGRAMMING IN "C" PRACTICAL	Hours / Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C309.1	Familiarize assignment, conditional statements.
C309.2	Validate looping statements.
C309.3	Familiarize simple electrical laws using C.
C309.4	Validate functions and structures in C.

Course Outcome linkage to Cognitive Level:

On successful completion of the course, the students will be able to attain following Course Outcomes

Course Outcome		Experiment linked	CL	Linked PO	Teaching Hrs
C309.1	Familiarize assignment, conditional statements	1,2,4,8,11	R,U,A	2,3,4	25
C309.2	Validate looping statements	3	U,A	2,3,4	5
C309.3	Familiarize simple electrical laws using C	5,9,10,12,13, 14,15,16	U,A	2,3,4	35
C309.4	Validate functions and structures in C	6,7	U,A	3,4	10
			Total sessions		**75**

Legends: R = Remember U= Understand; A= Application and above levels (Bloom's revised taxonomy)

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
PROGRAMMING IN "C" PRACTICAL	**--**	**3**	**3**	**3**	**--**	**--**	**--**

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LIST OF EXERCISES

1. Write C language program to find the solution of a quadratic equation.
2. Write C language program to find whether the given number is a positive number, negative number or zero.
3. Write C language program to find the sum of series using While loop.
4. Write C language program to perform the Arithmetic operation based on the numeric key press using switch case statement. (1-Addition, 2-Subtraction, 3-multiplication, 4 - Division).
5. Write C language program to implement Ohms Law.
6. Write C language program to find factorial of given N numbers using function.
7. Write C language program to prepare the total marks for N students by reading the Name, Reg.No, Marks 1 to Marks 6 using array of structure.
8. Write C language program to swap the values of two variables.
9. Write C language program to calculate the equivalent resistance of three resistances connected in series and parallel.
10. Write C language program to calculate the equivalent Capacitance of three Capacitors connected in series and parallel.
11. Write a simple C language program to print the address of a variable using pointer.
12. Write C language program to find Resonant Frequency of RLC Series and Parallel Circuits.
13. Write C language program to find the power factor of series RL circuits.
14. Write C language program to find the Q factor for series and parallel resonant circuits.
15. Write C language program to draw the symbol of NPN transistor using Graphics.
16. Write C language program to draw the symbol of Diode using Graphics.

LIST OF EQUIPMENTS

HARDWARE REQUIRMENT:

Desktop/laptop computers : 40 Nos.

Laser printer : 03 nos.

SOFTWARE REQUIREMENT:

C - Compiler and editor

Detailed Allocation of Marks for External Assessment

PROGRAMMING IN "C" PRACTICAL		
SL.NO.	**ALLOCATION**	**MARKS**
1.	Writing Algorithm	20
2.	Writing Program	20
3.	Execution Program	25
4.	Result	05
5.	Viva-voce	05
Total		**75**

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N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC401

Term : III

Course Name : CCTV & SECURITY SYSTEMS PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
CCTV & SECURITY SYSTEMS PRACTICAL	Hours / Week	Hours / Term	Marks			Duration
	4	60	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C401.1	Set up a CCTV system with cameras using DVR
C401.2	Set up a CCTV system using wireless link with LED interfacing
C401.3	Install a Biometric based security systems and access control models
C401.4	Install a Fire alarm unit.

Course Outcome linkage to Cognitive Level:

On successful completion of the course, the students will be able to attain following Course Outcomes

Course Outcome		Experiment linked	CL	Linked PO	Linked PSO	Teaching Hrs
C401.1	Set up a CCTV system with cameras using DVR	**1,2,3,4,5,6**	**U,A**	1,2,5	2	18
C401.2	Set up a CCTV system using wireless link with LED interfacing	**7,8,9**	**U,A**	1,2,5	2	18
C401.3	Install a Biometric based security systems and access control models	**10,11,12,13,14,15**	**U,A**	1,3,5	2	18
C401.4	Install a Fire alarm unit.	**16**	**A**	1,3,5	2	6
			Total sessions			**60**

Legends: R = Remember U= Understand; A= Application and above levels (Bloom's revised taxonomy)

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
CCTV & SECURITY SYSTEMS PRACTICAL	**3**	**3**	**2**	**-**	**3**	**-**	**-**

Course-PSO Attainment Matrix:

Course Name	Programme Specific Outcomes	
	1	2
CCTV & SECURITY SYSTEMS PRACTICAL	**-**	**3**

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CCTV & SECURITY SYSTEMS PRACTICAL

LIST OF EXERCISES

CYCLE-1

1. Set up a CCTV system with 1 camera connected to a monitor using single cable.
2. Set up a CCTV system with 4 cameras connected to a monitor with automatic switching.
3. Set up a CCTV system with 4 cameras connected to a DVR with recorded play back.
4. Set up a CCTV system with 4 cameras with DVR and configure a monitor through LAN.
5. Set up a CCTV system with 4 cameras with DVR and interface with a wall mounted LED TV to display a four channel outputs.
6. Checking the clarity and picture quality of different types of camera's by recording using 4 port DVR with 4 different cameras.
7. Set up a CCTV system with 4 cameras connected to a monitor using NVR with playback recording and automatic switching.
8. Set up a CCTV system with 4 cameras connected to a monitor using NVR and interface with wall mounted LED TV to view 4 channel outputs.
9. Study of PTZ camera.

CYCLE-2

10. Install and check the operation of RF ID based security system.
11. Install and check the operation of Bio-metric based finger print access control.
12. Install and check the operation of Bio-metric based Face-Recognizing access control.
13. Install and check the operation of RF ID & finger print based security system.
14. Install a Burglar alarm system.
15. Install a Video Door Phone (VDP) alarm system.
16. Install a Fire alarm unit in the given area.

EQUIPMENTS / COMPONENTS REQUIRED

Sl. No.	Name of the Equipments	Required Nos.
1	Camera	10
2	DVR	10
3.	NVR	10
4.	Monitor	10
5	Bio metric Access control kit	1
6	RFID Access control kit	1
7	Video Door Phone	1
8	Fire Alarm Kit	1

Scheme of valuation in TEE		
1.	CIRCUIT DIAGRAM	20
2.	CONNECTION	20
3.	EXECUTION & HANDLING OF EQUIPMENT	20
4.	OUTPUT / RESULT	10
5.	VIVA-VOCE	05
	Total	**75**

VIRUDHUNAGAR S.VELLAICHAMY NADAR POLYTECHNIC COLLEGE (AUTONOMOUS)

(Affiliated to Directorate of Technical Education, Chennai-25)

VIRUDHUNAGAR – 626 001

N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC302

Term : IV

Course Name : Industrial Electronics

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
Industrial Electronics	Hours / Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Time in Hrs
1	POWER DEVICES AND TRIGGER CIRCUITS	15
2	CONVERTERS AND CHOPPERS	15
3	INVERTERS & CYCLO CONVERTERS	15
4	APPLICATIONS OF POWER ELECTRONICS	15
5	SOLAR APPLICATIONS	15
	Total	75

Course Outcomes:

On successful completion of the course, the student will be able to:

C302.1	Understand the working of different types of Power electronic devices and circuits.
C302.2	Comprehend the various types of Power electronics circuits – Converters & Chopper.
C302.3	Learn about Inverters and Cycloconverters.
C302.4	Elucidate the applications of Power Electronic circuits.
C302.5	Know the applications of Solar energy .

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Teaching Hrs
C302.1	Understand the working of different types of Power electronic devices and circuits.	***R/U***	1,2	15
C302.2	Comprehend the various types of Power electronics circuits – Converters & Chopper.	***R/U***	1,2,5	15
C302.3	Learn about Inverters and Cycloconverters	***R/U***	1,2	15
C302.4	Elucidate the applications of Power Electronic circuits.	**U/A**	1,3,5	15
C302.5	Know the applications of Solar energy.	***R/U/A***	1,5,7	15
		Total sessions		75

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	POWER DEVICES AND TRIGGER CIRCUITS	15	25	***2***	***18***	***5***	*17.86*
II	CONVERTERS AND CHOPPERS	15	25	***2***	***18***	***5***	*17.86*
III	INVERTERS & CYCLO CONVERTERS	15	25	***2***	***18***	***5***	*17.86*
IV	APPLICATIONS OF POWER ELECTRONICS	15	25	***2***	***18***	***5***	*17.86*
V	SOLAR APPLICATIONS	15	25	***2***	***18***	***5***	*17.86*
I to V			15	***6***	***9***	***0***	*10.70*
	Total		**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
INDUSTRIAL ELECTRONICS	**3**	**2**	**1**	**-**	**3**	**-**	**1**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**POWER DEVICES AND TRIGGER CIRCUITS** **POWER DEVICES** Thyristor family –Working principle, VI characteristics and applications of SCR – Definitions for holding current, latching current, dv/dt rating, di/dt rating. Insulated gate bipolar transistor (IGBT), MOSFET and GTO - Symbol, principle of working, VI characteristics and applications. Comparison between power MOSFET, power transistor and power IGBT. **TRIGGER CIRCUITS** Triggering of SCR - Gate triggering –Types – Concepts of DC triggering, AC triggering, Pulse gate triggering – Pulse transformer in trigger circuit – Electrical isolation by opto isolator – Resistance capacitor firing circuit and waveform, Synchronized UJT triggering (ramp triggering) circuit and waveform.	15
II	**CONVERTERS AND CHOPPERS** (Qualitative treatment only) **CONVERTERS** Converters – Definition – Single phase Half controlled bridge converter with R load and RL load - importance of flywheel diode – Single phase fully controlled bridge converter with resistive load – voltage and current waveforms – Single phase fully controlled bridge converter with RL load – voltage and current waveforms Commutation- Natural commutation – Forced commutation – Types **CHOPPERS** Chopper – Definition –principle of DC chopper operation – Typical chopper circuit (Jones chopper) –Applications of DC chopper – Principle of working of single phase AC chopper - Chopper using MOSFET.	15
III	**INVERTERS & CYCLO CONVERTERS** **INVERTERS:** Inverter - Definition -Requirement of an inverter –Single phase bridge inverter with resistive load – Single phase bridge inverter with RL load –Methods to obtain sine wave output from an inverter- Output voltage control in inverters - McMurray inverter – advantages - Parallel inverter using IGBT. Battery Bank. **AC Voltage Controllers** Principle of Phase Control – Operation of Single phase AC voltage controllers with Resistive Load **CYCLO CONVERTERS** Definition – Operation of Single Phase Cyclo Converters with resistive load	15

IV	**APPLICATIONS OF POWER ELECTRONICS** Switch Mode Power Supplies — Uninterrupted Power Supply – Online (No Break) and OFF line (Short-Break) types – Static AC Circuit Breaker – AC Solid State Relays - High Frequency Fluorescent Lighting – Induction Heating – Electric Welding – High Voltage DC Transmission – Wind and Small Hydro Interconnection – Static VAR Compensators – Thyristor Controlled Inductors – Thyristor Switched Capacitors	15
V	**SOLAR APPLICATIONS** **SOLAR BASIC PRINCIPLES:** Definition : Solar Constant, Irradiance, Insolation, Peak Sun, Air Mass. Basic Principle of Photo-Voltaic Effect – Working of solar cell – Series and Parallel combination of PV module- IV and PV Characteristics of PV module. **Solar energy collectors** – Classifications – Flat plate collectors – Concentrating collectors – Parabolic Trough Concentrator, Parabolic Dish Concentrator - Solar Tower. **SOLAR THERMAL ENERGY APPLICATIONS:** Domestic Water Heating – Solar Cooking – Crop Drying – Active Solar Heating – Solar refrigeration and air conditioning systems.	15

Text Book:

1. Power Electronics by M.D. Singh – Tata McGraw Hill Publication.

Reference Book:

1. Industrial & Power Electronics By Harish C.Rai, Umesh Publication, 5th Edition 1994.
2. Power Electronics by M.H.Rashid - PHI Publication-3rd Edition-2005.
3. Industrial Electronics and control by Biswanath Paul –PHI publications- 2nd Edition - 2010.
4. Power Electronics by Dr.P.S.Bimbhra, Khanna publishers -2nd Edition- 1998.
5.Solar Energy: The physics and engineering of photovoltaic conversion, technologies and systems by Amo Smets,Klaus Jager,Olindo Isbella,Rene van Swaaij,Miro Zeman ,Uit publications.
6.Solar Energy: An Introduction by Michael E.Mackay ,1st Edition Oxford publications.
7. Photovoltaic Solar Energy from fundamentals to Applications by Angale reinders, Pierre Verlinden,Wilfried van Sark,Alexandre Freundlich Spi Global ,Pondicherry, India.

MODEL QUESTION PAPER – I

Term : III Time : 3hrs

Programme : Diploma in Electronics and Communication Engineering Max. Marks :75

Course : Industrial Electronics Course Code : N1EC302

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define Latching current.
2. Draw the symbols for (i) SCR (ii) IGBT.
3. What is Chopper?
4. Give any two requirements of Inverter.
5. What is ac Voltage Controller ?
6. What is photo voltaic effect?
7. List any two types of thermal collector.
8. Define commutation.

PART – B

9. Explain the working of opto coupler.
10. Draw the characteristics of GTO.
11. What is the effect of freewheeling diode in converters?
12. List the types of forced commutation.
13. List the methods of obtaining sine wave output from an inverter.
14. Explain Static AC Circuit Breaker.
15. Explain the effect of connecting solar cells in series.
16. Explain the working of solar cell.

[Turn over …..

PART – C

17. (a) Explain the principle of working and VI characteristics of SCR.

(Or)

(b) Explain the working of Synchronized UJT Triggering Circuit with the diagram.

18. (a) Explain the working of Single Phase Fully Controlled Bridge Converter with resistive load.

(Or)

(b) Explain the working of Jones Chopper.

19. (a) Explain the working of Mc Murray Inverter.

(Or)

(b) Explain the working of AC Voltage Controller.

20. (a) Explain the block diagram of SMPS.

(Or)

(b) Explain the working of Induction Heating.

21. (a) Explain the working of solar cell.

(Or)

(b) Explain the following (i) Solar Tower (ii) Solar cooker

MODEL QUESTION PAPER – II

Term : III Time : 3hrs

Programme : Diploma in Electronics and Communication Engineering Max. Marks :75

Course : Industrial Electronics Course Code : N1EC302

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define holding current.
2. Draw the symbols for (i) MOSFET (ii) GTO.
3. What is AC Chopper?
4. Give any two applications of Inverter.
5. What is CycloConverter?
6. Define Solar Constant?
7. Classify Solar Energy Collector.
8. List the types of commutation.

PART – B

9. Explain the working of opto coupler.
10. Draw the characteristics of SCR.
11. What are the advantages of freewheeling diode in converters?
12. List the types of forced commutation.
13. List the methods to control the output voltage of inverter.
14. Explain AC Solid State Relay.
15. Explain the effect of connecting solar cells in parallel.
16. Explain the working of solar cell.

[Turn over …..

PART – C

17. (a) Explain the principle of working and VI characteristics of MOSFET.

(Or)

(b) Explain the working of RC Triggering Circuit with the diagram.

18. (a) Explain the working of Single Phase Half Controlled Bridge Converter with resistive load.

(Or)

(b) Explain the working of Jones Chopper.

19. (a) Explain the working of Single Phase Bridge Inverter with resistive Load.

(Or)

(b) Explain the working of AC Voltage Controller.

20. (a) Explain the block diagram of on line UPS.

(Or)

(b) Explain the working of Static VAR Compensator.

21. (a) Explain the basic principle of Photo Voltaic Effect.

(Or)

(b) Explain the following (i) Solar Parabolic Trough Concentrator
(ii) Crop Drying

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VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC206

Term : IV

Course Name : COMMUNICATION ENGINEERING

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
COMMUNICATION ENGINEERING	Hours / Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Hours
I	AMPLITUDE MODULATION	15
II	ANGLE AND PULSE MODULATION	15
III	NETWORKS, ANTENNA AND PROPAGATION	15
IV	AUDIO SYSTEMS	15
V	DIGITAL CODES AND MODULATION	15
	Total	75

Course Outcomes:

On successful completion of the course, the student will be able to:

C206.1	Understand AM Transmitters and Receivers.
C206.2	Understand FM Transmitters and Receivers.
C206.3	Understand Networks,Antenna and Propagation.
C206.4	Understand Audio Systems.
C206.5	Understand Digital Communication and Coding.

Course Outcome Linkage to Cognitive Level:
Cognitive Level Legend: R- Remember, U- Understand, A- Application.

Course Outcome		CL	Linked PO	Teaching Hrs
C206.1	Understand AM Transmitters and Receivers.	**R/U/A**	1,2	15
C206.2	Understand FM Transmitters and Receivers.	**R/U/A**	1,2	15
C206.3	Understand Networks, Antenna and Propagation.	**R/U/A**	1,2,4,5,7	15
C206.4	Understand Audio Systems.	**R/U/A**	1,2,3	15
C206.5	Understand Digital Communication and Coding.	**R/U/A**	1,2,5	15
		Total sessions		75

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	AMPLITUDE MODULATION	15	25	***2***	***18***	***5***	*17.86*
II	ANGLE AND PULSE MODULATION	15	25	***2***	***18***	***5***	*17.86*
III	NETWORKS, ANTENNA AND PROPAGATION	15	25	***2***	***18***	***5***	*17.86*
IV	AUDIO SYSTEMS	15	25	***2***	***18***	***5***	*17.86*
V	DIGITAL CODES AND MODULATION	15	25	***2***	***18***	***5***	*17.86*
I to V*			15	***6***	***9***	***0***	*10.70*
	Total	75	**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
Communication Engineering	**3**	**3**	**1**	**1**	**1**	**-**	**1**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**AMPLITUDE MODULATION** **1.1 MODULATION**: Frequency spectrum. Relationship between wavelength and frequency, Need for modulation, types of modulation. **1.2 AMPLITUDE MODULATION:** Expression, AM spectrum and sidebands, types of AM systems - balanced modulator. SSB generation – phase shift and filter methods, advantages and disadvantages of SSB. AM VSB system. Diode detector. **1.3 AM TRANSMITTER:** Types of transmitters - high level AM transmitter and low level AM transmitter. SSB transmitter. **1.4 AM RECEIVER:** TRF receiver, super heterodyne radio receiver- Selection of IF- Image frequency and rejection- AGC types, SSB receiver.	15
II	**ANGLE AND PULSE MODULATION** **2.1 FREQUENCY MODULATION:** Expression - waveforms - frequency spectrum, effects of noise in FM, comparison of AM and FM, varactor diode modulator. **2.2 FM DETECTORS:** Balanced Slope detector, phase discriminator, ratio detector (Qualitative treatment only) **2.3 FM TRANSMITTER & RECEIVER:** Direct and Indirect methods- stereophonic FM transmitter. FM receiver- Block diagram – AFC-stereophonic FM receiver. **2.4 PHASE MODULATION :** Principles, phase modulator circuit, comparison between FM and PM. **2.5 PULSE MODULATION:** Types, sampling theorem. Generation and detection of PAM, PWM, PPM,PCM.	15
III	**NETWORKS, ANTENNA AND PROPAGATION** **3.1 NETWORKS (QUALITATIVE TREATMENT ONLY):** Symmetrical and asymmetrical networks –electrical characteristics of symmetrical network -characteristic impedance using Zoc and Zsc (T & Pi network only)-propagation constant(definition only)-asymmetrical network – electrical characteristics – matching network. **3.2 EQUALIZER:** Types, applications-constant resistance equalizer. **3. 3ATTENUATOR:**	15

	Types - symmetrical T and Pi attenuators – simple problems – variable attenuators. **3.4 FILTERS:** Types and definitions – circuit elements and cutoff frequencies of LPF, HPF (only simple problems). **3.5 TRANSMISSION LINES:** Transmission line equivalent circuit- primary and secondary constants, Travelling and standing waves, SWR, waveguides- types, advantages. **3.6 ANTENNAS:** Basic antenna principle, polarization, directive gain, directivity, radiation pattern, driven array - broad-side and end-fire array- parasitic array, folded dipole, Yagi antenna, parabolic antenna. **3.7 PROPAGATION (SHORT THEORY ONLY) :** Ground wave propagation, space wave propagation, ionospheric layers - sky wave propagation.	
IV	**AUDIO SYSTEMS** **4.1 MICROPHONES:** (QUALITATIVE TREATMENT ONLY) Construction and performance of the following microphones: carbon, condenser, piezo-electric, moving coil and velocity ribbon. **4.2 LOUD SPEAKERS:** Constructional details of dynamic cone type, Horn type and electro-static loud speakers, woofer, midrange and tweeter, cross-over network. Surround-sound systems. **4.3 AUDIO RECORDING AND REPRODUCTION:** Compact disc system- MP3 system - DVD system - Stereophonic system - Hi-Fi system principles- Dolby –DTS.	15
V	**DIGITAL CODES AND MODULATION** **5.1 CHARACTERISTICS OF DIGITAL TRANSMISSION** : Comparison of analog and digital signals – Advantages of digital signal processing - Characteristics of data transmission circuits -Bandwidth requirement – speed - Baud rate- Noise- Crosstalk- Distortion – Equalizers. **5.2 DIGITAL CODES** : ASCII Code – EBCDIC Code - Error detection codes – Parity check codes – Redundant codes - Error correction – Retransmission- forward error correcting code – Hamming code. **5.3 DIGITAL MODULATION TECHNIQUES** : ASK, FSK, PSK, modulation and demodulation techniques (only block diagram and operation and bandwidth), comparison.	15

Text Book:-

1. Electronic communication Systems – Kennedy – TMH.
2. Principles of Communication Engineering -Anokh Singh,A.K.Chhabra-S.Chand &Co.
3. Fundamentals of Acoustics – Kingsler & Frey – Wiley Eastern Ltd.

Reference Book:-

1. Networks lines and fields – John D.Ryder, PHI.
3. Electronic Communication – Dennis Roddy and John colen – PHI.
5. Communication Electronics – Principles & Applications – Louis.E.Frenzel, TMH.

MODEL QUESTION PAPER-I

Term : IV Time : 3 Hrs

Programme : Diploma in Electronics and Communication Engineering Max Marks:75

Course : Communication Engineering Course Code : N1EC206

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define modulation index for AM.
2. Define AGC.
3. Define frequency modulation.
4. What is the advantage of FM over AM?
5. What is an attenuator?
6. Define symmetrical network.
7. Define microphone.
8. What is FSK?

PART - B

9. What is the Need for Modulation ?
10. Mention the Types of AM-Transmitter.
11. What is AFC?
12. What are the Types of Pulse Modulation ?
13. Define:- Propagation Constant.
14. What are the Types of Antenna?
15. Differentiate Tweeter and Woofer.
16. Write Notes on DTS.

[Turn over …..

PART – C

17. a) What is the need for modulation? Derive expression for AM signal.

(or)

b) Explain Super Heterodyne Receiver with block diagram.

18. a) i) Explain the working of a Ratio detector with circuit diagram.
ii) Compare AM & FM.

(or)

b) Explain generation and demodulation of PWM.

19. a) Derive the expression for the cut-off frequency and circuit elements of constant-k LPF.

(or)

b) Write notes on different types of propagation.

20. a) Explain the working of carbon microphone with Constructional details.

(or)

b) Describe about MP-3 System.

21. a) Draw the fundamental block diagram of digital communication system and explain. State the advantages of digital communication.

(or)

b) With a neat diagram explain FSK modulation & demodulation.

MODEL QUESTION PAPER – II

Term : IV Time : 3 Hrs

Programme : Diploma in Electronics and Communication Engineering Max Marks: 75

Course : Communication Engineering Course Code : N1EC206

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define Amplitude Modulation.
2. Give the Advantages of SSB.
3. What is the Effect of Noise,in FM?
4. What are the Types of Pulse Modulation?
5. Define Characteristic Impedance.
6. Mention the Types of Antenna,
7. What are the Types of Loud Speaker?
8. Define:- Baud Rate.

PART - B

9. Derive the Relationship between Wave Length & Frequency.
10. Compare Delayed AGC and Simple AGC.
11. Differentiate between FM and PM.
12. Sketch the Diagram of PWM Generation.
13. Draw the High Pass Filter and Write the Formula for Fc.
14. Write Short Notes on Yagi Antenna.
15. Write Short Notes on Cross Over Network.
16. What is Error Correction Code?

[Turn over …..

PART – C

17. a) Explain about High Level AM Transmitter, with Block Diagram.

(Or)

b) Draw and Explain.SSB Receiver.

18. a) Explain Stereophonic FM Transmitter, with Diagram.

(Or)

b) Explain the Generation and Detection of PAM.

19. a) Explain the Electrical Characteristics of Symmetrical Network.

(Or)

b) Draw and explain about Broad Side Array and End Fire Array.

20. a) Describe about Dynamic Cone Type Loud Speaker.

(Or)

b) Explain DVD System, with Neat Diagram.

21. a) Explain Briefly about Error Correction Code.

(Or)

b) Discuss about Propagation and its types.

VIRUDHUNAGAR S.VELLAICHAMY NADAR POLYTECHNIC COLLEGE

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VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC207

Term : IV

Course Name : DIGITAL ELECTRONICS

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
	Hours / Week	Hours / Term	Marks			Duration
DIGITAL ELECTRONICS	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Time in Hrs
1	NUMBER SYSTEM, BOOLEAN ALGEBRA,	15
2	COMBINATIONAL CIRCUITS	15
3	SEQUENTIAL CIRCUITS	15
4	MEMORY DEVICES	15
5	MICRO PROCESSOR -8085	15
	Total	**75**

Course Outcomes:

On successful completion of the course, the student will be able to:

C207.1	Familiarize the number systems and types of codes and understand the basic logic gates.
C207.2	Apply the basic knowledge of digital electronics to design simple combinational logic circuits.
C207.3	Understand sequential logic circuits and distinguish various types of flipflops
C207.4	Understand the functions and applications of various types of memories.
C207.5	Understand the architecture and familiarize various Instructions in 8085.

Course Outcome linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		**CL**	**Linked PO**	**Linked PSO**	**Teaching Hrs.**
C207.1	Familiarize the number systems and types of codes and understand the basic logic gates.	**R/U/A**	1,2,3	-	15
C207.2	Apply the basic knowledge of digital electronics to design simple combinational logic circuits.	**R/U/A**	1,2,3	-	15
C207.3	Understand sequential logic circuits and distinguish various types of flip flops	**R/U/A**	1,2,3	-	15
C207.4	Understand the functions and applications of various types of memories.	**R/U/A**	1,2	1	15
C207.5	Understand the architecture and familiarize various Instructions in 8085.	**R/U/A**	1,2,5	1	15
		Total sessions			75

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	Familiarize the number systems and types of codes and understand the basic logic gates.	15	25	**2**	**18**	**5**	17.86
II	Apply the basic knowledge of digital electronics to design simple combinational logic circuits.	15	25	**2**	**18**	**5**	17.86
III	Understand sequential logic circuits and distinguish various types of flipflops	15	25	**2**	**18**	**5**	17.86
IV	Understand the functions and applications of various types of memories.	15	25	**2**	**18**	**5**	17.86
V	Understand the architecture and familiarize various Instructions in 8085.	15	25	**2**	**18**	**5**	17.86
I to V *			15	**6**	**9**	**0**	10.70
	Total	75	**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
DIGITAL ELECTRONICS	**3**	**3**	**3**	**-**	**1**	**-**	**-**

Course-PSO Attainment Matrix:

Course Name	Programme Specific Outcomes	
	1	2
DIGITAL ELECTRONICS	**2**	**-**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**NUMBER SYSTEM, BOOLEAN ALGEBRA, LOGIC GATES AND DIGITAL LOGIC FAMILIES** Binary, Octal, Decimal, Hexadecimal - Conversion from one to another. Binary codes – BCD code, Gray code, Excess 3 code. Boolean Algebra - Boolean postulates and laws - De-Morgan's theorem - Simplification of Boolean expressions using Karnaugh map (up to 4 variables-pairs, quad, octets) - Don't care conditions and constructing the logic circuits for the Boolean expressions. **LOGIC GATES AND DIGITAL LOGIC FAMILIES:-** Gates – AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR - Implementation of logic functions using gates - Realization of gates using universal gates - Simplification of expression using Boolean techniques- Boolean expression for outputs. Digital logic families – Fan in , Fan out, Propagation delay - TTL,CMOS Logics and their characteristics - comparison and applications -Tristate logic.	15
II	**COMBINATIONAL CIRCUITS:-** Arithmetic circuits - Binary – Addition, subtraction, 1's and 2's complement - Signed binary numbers- Half Adder- Full Adder - Half Subtractor - Full Subtractor - Parallel and serial Adders - BCD adder. Encoder and decoder – 3 to 8 decoder, BCD to seven segment decoder – Multiplexer - basic 2 to 1 MUX, 4 to 1 MUX, 8 to 1 MUX - applications of the MUX – Demultiplexer - 1 to 2 demultiplexer, 1 to 4 demultiplexer, 1 to 8 demultiplexer - Parity Checker and generator.	15
III	**SEQUENTIAL CIRCUITS:** FLIP FLOPS – SR, JK, T, D FF, JK- MS FF - Triggering of FF – edge & level , Counters – 4 bit Up - Down Asynchronous / ripple counter - Decade counter- Mod 3, Mod 7 counter. 4 bit Synchronous Up - Down counter - Johnson counter, Ring counter **REGISTERS** 4-bit shift register - Serial IN Serial OUT - Serial IN Parallel OUT - Parallel IN Serial OUT - Parallel IN Parallel OUT	15
IV	**MEMORY DEVICES:-** Classification of memories - RAM organization - Address Lines and Memory Size - Read /write operations - Static RAM - Bipolar RAM cell- Dynamic RAM - SD RAM - DDR RAM. Read only memory – ROM organization - Expanding memory – PROM – EPROM and EEPROM - Flash memory - Anti Fuse Technologies.	15
V	**MICROPROCESSOR – 8085:-** Evolution of microprocessor 8085 – Architecture of 8085- Instruction sets - Addressing modes - Memory mapped I/O and I/O mapped I/O and its Comparison. Machine cycle – Opcode fetch - memory read - memory write - I/O read, I/O write - Instruction cycle Timing diagram for LDA, STA, IN, OUT instruction. Interrupts (types & Priorities**)**	15

Text Book:

1. Principles of Digital Electronics – K. Meena – PHI Publications 2011.

Reference Book:

1. Digital Principles & Applications – Albert Paul Malvino & Donald P.Leach – TMH.
2. Digital Electronics – William H.Gothmann – Prentice Hall of India.
3. Modern Digital Electronics – R.P. Jain – TMH.
4. Digital Electronics – Roger L. Tokheim Macmillan – McGraw – Hill.
5. Microprocessor architecture, programming and application – Ramesh S. Gaonkar – Wiley eastern limited.
6. Introduction to Microprocessor – ADITYA P MATHUR-Tata McGraw-Hill publishing Company Limited.

MODEL QUESTION PAPER - I

Term : IV Time : 3Hrs

Programme : Diploma in Electronics and Communication Engineering Max.Marks :75

Course : Digital Electronics Code : N1EC207

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.
(2) Answer division (a) or division (b) of each question in PART – C.
(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define fan in and fan out.
2. Calculate the 2's complement of 01101110.
3. Define Flip-flop.
4. What are the modes available in shift register?
5. Mention the types of memory.
6. State machine cycle.
7. Define interrupt.
8. Convert $(28)_{10}$ into binary.

PART – B

9. Construct the logic circuit for $\bar{A}B + A\bar{B}$.
10. Explain half adder.
11. Write short notes on parity checker.
12. Explain ROM organization.
13. Explain anti fuse technology.
14. Explain memory mapped I/O and I/O mapped I/O.
15. What are the addressing modes of 8085?
16. Explain the working of AND gate.

[Turn over …..

PART – C

17. a) (i) Convert $(10101101)_2$ into decimal.
(ii) Simplify the following function using K map $Y = \Sigma\, m(0,2,4,6,8,10,12,14)$

(Or)

b) Realize logic gates using NAND gates.

18. a) Explain the operation of BCD to 7 segment Decoder.

(Or)

b) Explain the operation of half subtractor and full adder.

19. a) With neat diagram and explain the circuits of SR and JK flip flop.

(Or)

b) With neat diagram explain the operation of ring counter.

20. a) Explain Static RAM Cell.

(Or)

b) Explain EEPROM.

21. a) Explain the addressing modes of 8085.

(Or)

b) Explain timing diagram for LDA address instruction.

MODEL QUESTION PAPER - II

Term : IV Time : 3hrs

Programme : Diploma in Electronics and Communication Engineering Max. Marks: 75

Course : Digital Electronics Code : N1EC207

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.
(2) Answer division (a) or division (b) of each question in PART – C.
(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Draw EX-OR gate with its truth table.
2. What is mean by Parity Checker?
3. Define Counter
4. What is mean by PISO shift register?
5. Explain EEPROM
6. State machine cycle.
7. Define interrupt.
8. What is mean by Excess 3 code?

PART – B

9. Explain Tristate gate.
10. Explain half subtractor.
11. Write short notes on parity generator.
12. Explain RAM organization.
13. Explain Flash memory.
14. Explain memory mapped I/O and I/O mapped I/O.
15. How instruction set is classified in 8085.
16. Explain the working of NOR gate.

[Turn over …..

PART – C

17. a) (i) Explain De-Morgan's theorem
(ii) Simplify the following function using K map $Y = \Sigma\, m(1,5,6,7,11,12,13,15)$

(Or)

b) Realize logic gates using NOR gates.

18. a) Explain the operation of BCD to 7 segment Decoder.

(Or)

b) Explain the operation of BCD adder.

19. a) With neat diagram and explain the circuits of T and D flip flop.

(Or)

b) With neat diagram explain the operation of Johnson counter.

20. a) Explain Bipolar RAM Cell.

(Or)

b) i) Explain EPROM.
ii) Explain Anti fuse technology.

21. a) Draw and explain the architecture of 8085.

(Or)

b) Explain timing diagram for STA address instruction.

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(Affiliated to Directorate of Technical Education, Chennai-25)

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N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC303

Term : IV

Course Name : LINEAR INTEGRATED CIRCUITS

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
Linear Integrated Circuits	Hours/ Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Time in Hrs
1.	Introduction to Operational Amplifiers	15
2.	Opamp applications	15
3.	PLL & Applications	15
4.	D/A and A/D converters	15
5.	Special Functions ICs	15
	Total	75

Course Outcomes:

On successful completion of the course, the student will be able to:

Code	**Course Outcomes**
C303.1	Acquire Knowledge about Operational amplifier.
C303.2	Understand different applications based on operational amplifier.
C303.3	Understand PLL & demonstrate different applications based on it.
C303.4	Understand the operation of the most commonly used A/D, D/A converter types
C303.5	Acquire knowledge about timer IC and voltage regulator ICs

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome linkage to Cognitive Level:

Course Outcome		**CL**	**Linked PO**	**Linked PSO**	**Teaching Hrs**
C303.1	Acquire Knowledge about Operational amplifier	***R/U/A***	1,2	1	15
C303.2	Understand different applications based on operational amplifier	***R/A***	1,2,4,7	1	15
C303.3	Understand PLL & demonstrate different applications based on it.	***R/U/A***	1,2,3	1,2	15
C303.4	understand the operation of the most commonly used A/D, D/A converter types	***R/U/A***	1,2,5,7	1	15
C303.5	Acquire knowledge about timer IC and voltage regulator ICs	***R/U/A***	1,2	1	15
		Total sessions			75

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hour	Max. Marks per Unit	Questions to be set for			Marks weightage (%)
				R	U	A	
I	Introduction to Operational Amplifiers	15	25	**2**	**18**	**5**	17.86
II	Opamp applications	15	25	**2**	**18**	**5**	17.86
III	PLL & Applications	15	25	**2**	**18**	**5**	17.86
IV	D/A and A/D converters	15	25	**2**	**18**	**5**	17.86
V	Special Functions ICs	15	25	**2**	**18**	**5**	17.86
I to V*			15	**6**	**9**	**0**	10.70
	Total	75	**140**	**16**	**99**	**25**	**100**

***3 x 2 Marks and 3 x3 Marks from any unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
Linear Integrated Circuits	**3**	**3**	**1**	**1**	**1**	**-**	**3**

Course-PSO Attainment Matrix

Course	Programme Specific Outcomes	
	1	2
LINEAR INTEGRATED CIRCUITS	**3**	**1**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

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- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**INTRODUCTION TO OPERATIONAL AMPLIFIERS** Integrated circuit - Classification of IC - Advantages of IC over discrete components –Types of IC Packages - Operational amplifier IC 741 – Schematic symbol for opamp – pin diagram of IC 741 –Block diagram of an opamp – Characteristics of an Ideal opamp - Simple Equivalent circuit of an opamp – virtual ground – opamp parameters – CMRR – Slewrate. Basic linear circuits- Inverting Amplifier, Non Inverting amplifier – Differential Amplifier – sign changer – scale changer. (Simple problems).	15
II	**OPAMP APPLICATIONS** Summing amplifier- Multiplier – Divider – Voltage follower – comparator – zero crossing detector - Integrator – Differentiator – Voltage to current converter – current to voltage converter – Instrumentation amplifier. Waveform generators – square wave, triangular wave, sine wave, saw tooth wave generators. (Qualitative treatment only).	15
III	**PLL & APPLICATIONS (Qualitative treatment only)** PLL – Basic principles of PLL – Basic Block schematic of PLL – Lock range – capture range - -Basic components of PLL – Phase detector, LPF –VCO. Monolithic VCO 566- Pin diagram –Basic Block diagram of VCO 566. Monolithic PLL 565-Pin diagram - Functional Block diagram of PLL IC 565, Applications of PLL – frequency translation – frequency multiplication.	15
IV	**D/A AND A/D CONVERTERS** **D/A CONVERTERS** Digital to analog converter – Basics of D/A conversion –weighted Resistor D/A Converter – R-2R Ladder D/A Converter – Specifications of DAC-Accuracy, Resolution, Monotonocity, Settling time. **A/D CONVERTERS** Analog to digital converter – Basics of A/D conversion – sampling – Sample and hold circuit – quantization – Types of A/D converter – Block diagram of Flash, Successive approximation, Ramp, Dual Slope ADC – Specifications of ADC – Accuracy, Resolution, conversion time – Functional Block diagram of IC ADC 0808	15

V	**SPECIAL FUNCTION ICs: (qualitative treatment only)** IC 555 Timer – pin diagram of IC 555 – Functional Block diagram of IC555 – Applications – Astable multi vibrator – mono stable multi vibrator – Schmitt trigger. IC voltage regulators – linear fixed voltage regulator – Positive voltage regulator using IC 78xx, negative voltage regulator using IC 79xx General purpose regulator using LM 723-Pin diagram of LM723- Low voltage and High voltage regulator using LM 723.	15

Text Book:

1. Linear Integrated circuits – Roychoudhury&Shail.B. Jain – New age International
Publishers – II Edition – 2004.

2."Integrated circuits" – K.R. Botkar – KhannaPulbisher's – 1996

Reference Book:

1. Introduction to system design using IC "-B.S. Sonde – Wiley Eastern Limited– II Edition– 1992.

2."Operational Amplifiers and Linear Integrated circuits"- Ramakant. A Gayakwad
–Prentice Hall – 2000.

3. Digital Integrated Electronics –Taub&Schlling – Mcgraw Hill – 1997.

4. Operational amplifiers and Linear Integrated circuits by Robert F.Coughlin and Frederick F.Driscoll – PHI – publications –sixth Edition-2009.

5. Linear Integrated Circuits by Salivahanan &V.S.Kanchana Baskaran- TMH.

MODEL QUESTION PAPER - I

Term : IV Time : 3 Hrs

Programme : Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : Linear Integrated Circuits Course Code : N1EC303

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. State any two advantages of IC over discrete components.
2. Draw the pin diagram of operational amplifier.
3. Define voltage follower and draw its circuit diagram.
4. Draw the operational amplifier circuit for sign changer.
5. Define PLL and mention one application of PLL.
6. Mention the different types of ADC.
7. State the application of IC 555.
8. What is a Schmitt trigger?

PART – B

9. Draw and mention the pin details of IC 741.
10. Define slew rate and CMRR.
11. Explain comparator using operational amplifier.
12. Explain capture range of a PLL.
13. Draw functional Block diagram of PLL IC 565.
14. Define resolution and accuracy of DAC.
15. Draw the functional block diagram of IC 555 timer.
16. Draw the Negative voltage regulator circuit using IC 79XX.

[Turn over …..

PART – C

17. (a) (i) Draw the block diagram of an Op-Amp and explain.

(ii) Explain virtual ground concept.

(Or)

(b) Explain inverting amplifier and non-inverting amplifier using Op-Amp.

18. (a) Explain the operation of Op-Amp as instrumentation amplifier with diagram.

(Or)

(b) Explain the operation of Op-Amp as square wave generator with diagram.

19. (a) Explain the frequency translation and frequency multiplication using PLL with diagram.

(Or)

(b) Draw the pin diagram and block diagram of VCO 566 and explain.

20. (a) Draw the circuit diagram of R-2R ladder D/A converter and explain its operation.

(Or)

(b) Explain the successive approximation type analog to digital converter with neat diagram.

21. (a) Explain the operation of monostable multivibrator with neat circuit diagram.

(Or)

(b) Explain the operation of LM 723 as low voltage regulator with neat circuit diagram.

MODEL QUESTION PAPER - II

Term : IV Time : 3 Hrs

Programme : Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : Linear Integrated Circuits Course Code : N1EC303

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. What is op-amp. Draw its symbol.
2. Define slew rate of an op amp.
3. Draw the divider circuit using op amp.
4. Draw the square waveform generator using op amp.
5. List out basic components of PLL.
6. Mention the different types of ADC.
7. Draw the pin diagram of IC 555.
8. Define Monotonocity in DAC.

PART – B

9. What is Virtual ground in an operational amplifier?
10. Mention the characteristics of an op-amp.
11. Draw and explain the multiplier circuit using op amp.
12. Define lock range and capture range in PLL.
13. Draw the functional diagram of IC VCO 566.
14. Explain the basics of Digital to Analog conversion.
15. Briefly explain the process of ADC conversion.
16. Draw the functional block diagram of IC 555.

[Turn over …..

PART – C

17. (a) Explain inverting and non-inverting amplifier using op-amp.

(Or)

(b) Explain sign changer and scale changer using op-amp.

18. (a) Explain instrumentation amplifier using op-amp.

(Or)

(b) With neat diagram, explain the operation of saw tooth wave generator.

19. (a) Draw and explain the basic block diagram of PLL.

(Or)

(b) Explain the frequency translation and frequency multiplication using PLL with diagram.

20. (a) With neat diagram, explain the operation of Weighted Resistor DAC.

(Or)

(b) With neat diagram, explain dual slope ADC.

21. (a) With neat diagram, explain the operation of Schmitt Trigger using IC 555.

(Or)

(b) Explain the operation of low voltage regulator using LM 723.

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VIRUDHUNAGAR – 626 001

N1 - SCHEME

Programme : Diploma in Electronics and communication Engineering

Course code : N1EC210

Term : IV

Course Name : Industrial Electronics and Communication Engineering Practical

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
Industrial Electronics and Communication Engineering Practical	Hours / Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C210.1	Familiarize Inverters choppers and Commutation circuits
C210.2	Validate PLC, Cyclo converters and Solar principles
C210.3	Construct Basic circuits, low pass and high pass filters Circuits
C210.4	Examine the basic concepts of analog modulation schemes

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		Linked Expts.	CL	Linked PO	Teaching Hrs
C210.1	Familiarize Inverters choppers and	**1,2,3,4**	**U,A**	1,2	**15**
C210.2	Validate PLC, Cyclo converters and Solar principles	**5,6,7,8,9**	**R,U**	1,4,7	**20**
C210.3	Construct Basic circuits , low pass and high pass filters circuits	**10,11,14,18**	**R,U**	1,2,3	**18**
C210.4	Examine the basic concepts of analog modulation schemes	**12,13,15,16,17**	**R,U,A**	2,3,4	**22**
Total sessions					**75**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
INDUSTRIAL ELECTRONICS AND COMMUNICATION ENGINEERING PRACTICAL	**3**	**3**	**2**	**2**	**-**	**-**	**1**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

LIST OF EXERCISES

INDUSTRIAL ELECTRONICS PRACTICAL

1. Verify Phase control characteristics of SCR.
2. Construct and test commutation circuits of SCR.
3. Construct and test a MOSFET based PWM chopper circuit.
4. Construct a Series Inverter and obtain its output waveform.
5. Construct a Cyclo converter and obtain its output waveform.
6. Write and implement a simple ladder logic program using digital inputs and outputs for PLC.
7. Write and implement a simple ladder logic program using timer and counter in PLC.
8. I-V and P-V characteristics of series combination of PV modules.
9. I-V and P-V characteristics of parallel combination of PV modules.

COMMUNICATION ENGINEERING PRACTICAL

10. Construct attenuator & narrow band rejection filter (notch filter) and test its characteristics.
11. Construct and test active low pass filter & high pass filter.
12. Construct an AM modulator and Detector circuit and trace the output waveform and simulate it using simulation tool like PSPICE/ multisim/orcad/tina. (Simulation not for Examination)
13. Construct a FM modulator circuit and trace the output waveform and simulate it using simulation tool like PSPICE/ multisim/orcad/tina. (Simulation not for Examination).
14. Construct & test IF amplifier stage of super heterodyne receiver.
15. Construct and test PAM generation circuit and detection circuit.
16. Construct and test PWM generation circuit and detection circuit.
17. Construct and test PPM generation circuit and detection circuit.
18. Construct and test a three way crossover network.

MAJOR EQUIPMENTS REQUIRED

SL.NO.	Name of the Equipment	Range	Required Nos.
1.	Regulated power supply	0-30V	5
2.	Dual trace CRO	-	8
3.	Signal Generator	-	6
4.	Converter Kit using SCR	-	1
5.	Commutation Kit	-	1
6.	MOSFET Based PWM Chopper	-	1
7.	Series Inverter Kit	-	1
8.	PAM Kit	-	1
9.	PWM Kit	-	1
10.	PPM Kit	-	1
11.	PCM Kit	-	1
12.	PV module	-	2
13.	Cyclo converter kit	-	1

Scheme of valuation in TEE		
1.	Circuit Diagram	20
2.	Connection	25
3.	Execution & handling of equipment	15
4.	Result	10
5.	Viva-voce	05
	Total	**75**

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N1 - SCHEME

Programme : Electronics and Communication Engineering

Course code : N1EC310

Term : IV

Course Name : INTEGRATED CIRCUITS PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
INTEGRATED CIRCUITS PRACTICAL	Hours / Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C310.1	Familiarize different logic gate IC's
C310.2	Construct arithmetic, combinational, logic circuits
C310.3	Construct and analyze the Op-amp application circuits.
C310.4	Construct multivibrator circuits using 555 IC and power supply using IC 7805.

Course Outcome linkage to Cognitive Level:

On successful completion of the course, the students will be able to attain following Course Outcomes

Course Outcome		Experiment linked	CL	Linked PO	Linked PSO	Teaching Hrs
C310.1	Familiarize different logic gate IC's	**1, 2**	**R, U, A**	1,2,3	1	10
C310.2	Construct arithmetic, combinational, logic circuits	**3,4,5,6,7,8,9,10**	**R,U, A**	1,2,3	1	30
C310.3	Construct and analyze the Op-amp application circuits.	**11,12,13,14,18**	**R, U, A**	1,2,3	1	20
C310.4	Construct multivibrator circuits using 555 IC and power supply using IC 7805.	**15,16,17**	**R, U, A**	1,2,3	1	15
			Total sessions			**75**

Legends: R = Remember U= Understand; A= Application and above levels (Bloom's revised taxonomy)

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
INTEGRATED CIRCUITS PRACTICAL	**3**	**3**	**3**	**-**	**-**	**-**	**-**

Course-PSO Attainment Matrix:

Course Name	Programme Specific Outcomes	
	1	2
INTEGRATED CIRCUITS PRACTICAL	**3**	**-**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

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INTEGRATED CIRCUITS PRACTICAL

LIST OF EXERCISES

1. Verification of truth table of OR, AND, NOT, NOR, NAND, EX-OR gates.
2. Realization of basic gates using NAND & NOR gates.
3. Half adder, Full adder using ICs.
4. Half Subtractor, Full Subtractor using ICs.
5. Construction and verification of truth table for Decoder/Encoder.
6. Construction and verification of truth table for Multiplexer/De-multiplexer
7. Construction and verification of Parity Checker / Generator
8. Construction and verification of truth table for RS, D, T, JK, flip-flop.
9. Construct a Single digit Decade / 4 - bit Counter with 7 segment display.
10. Construct and test shift registers in SIPO mode using IC 74164.
11. Inverting Amplifier and Non inverting Amplifier with DC signal using op-amp.
12. Integrator and Differentiator using op-amp.
13. Summing amplifier & Differential amplifier using op-amp.
14. Comparator and Schmitt trigger circuit using op-amp IC-741.
15. Astable Multivibrator using IC 555.
16. Monostable Multivibrator using IC 555.
17. Construction of simple power supply using IC 78XX.
18. DAC using R-2R network.
19. Study of simulation of logic gates, inverting and non inverting, voltage follower, integrator, differentiator, summing amplifier, differential amplifier using PSPICE/multisim/orcad/tina (Not for examination)

EQUIPMENTS/COMPONENTS REQUIRED

EQUIPMENTS

Sl. No.	Name of the Equipments	Required Nos.
1	Digital Trainer Kit	10
2	Function Generator	2
3	0-30 V power supply	2
4	20 MHz CRO	2

COMPONENTS

Sl. No.	Name of the Components	Required Nos.
1.	IC7400, IC7402, IC7404, IC7408, IC7432, IC7486	10
2.	IC 74180, IC 74153, IC 7476, IC 7474	10
3.	IC 7490, IC 7493, IC 7495	10
4.	IC 74147, IC 74138, IC 74151	10
5.	IC 555, IC 78XX	10

Scheme of valuation in TEE		
1.	Circuit Diagram	20
2.	Connection	25
3.	Execution & Handling of equipment	15
4.	Result	10
5.	Viva-voce	05
	Total	**75**

VIRUDHUNAGAR S.VELLAICHAMY NADAR POLYTECHNIC COLLEGE (AUTONOMOUS)

(Affiliated to Directorate of Technical Education, Chennai-25)

VIRUDHUNAGAR – 626 001

N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC402

Term : IV

Course Name : HOME APPLIANCES SERVICING AND ARDUINO PROGRAMMING PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
HOME APPLIANCES SERVICING AND ARDUINO PROGRAMMING PRACTICAL	Hours / Week	Hours / Term	Marks			Duration
	4	60	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C402.1	Interface input, output devices with the Arduino Board.
C402.2	Interface various sensors with the Arduino Board.
C402.3	Control DC Motor, DC geared motor, DC Servo motor using the Arduino Board.
C402.4	Assemble the various parts of domestic appliances and test its performances.

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		Linked Expts.	CL	Linked PO	Teaching Hrs
C402.1	Interface input, output devices with the Arduino Board.	**1,2,16**	U,A	1,4	10
C402.2	Interface various sensors with the Arduino Board.	**3,5,6,7,8**	U,A	1,2	20
C402.3	Control DC Motor, DC geared motor, DC Servo motor using the Arduino Board.	**4,5,7**	U,A	1,2,3	4
C402.4	Assemble the various parts of domestic appliances and test its performances.	**9,10,11,12,13,14,15**	U,A	1,5	26
		Total sessions			**60**

Legends: R = Remember U= Understand; A= Application and above levels (Bloom's revised taxonomy)

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
Home Appliances Servicing and Arduino Programming Practical	**3**	**2**	**1**	**1**	**3**	**-**	**-**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

LIST OF EXERCISES

PART A – ARDUINO PROGRAMMING

1. a) Write a Program in Arduino to blink an LED 10 times.
   b) Write a Program in Arduino to Turn ON an LED using Serial Read() command
2. Write a Program in Arduino to interface a Relay with the help of push button.
3. a) Write a Program in Arduino to vary the brightness of RGB LED.
   b) Write a Program in Arduino to measure the value of an LDR.
4. Write a Program in Arduino to run a DC geared motor and servo motor in forward and reverse Direction.
5. Write a Program in Arduino using Moisture Sensor to Turn ON a DC Motor when there is no moisture and Turn OFF a DC Motor when there is moisture.
6. Write a Program in Arduino to measure the distance using Ultrasonic sensor and turn ON a Buzzer when the distance is below 10 cm.
7. Construct an obstacle avoiding robot using Arduino.
8. Write a Program in Arduino to interface an IR Sensor.

PART B – HOME APPLIANCES SERVICING

9. Familiarization of tools used for electrical repair works and personal protection equipments.
10. Dismantling of Electrical iron box, identifying the parts, checking the conditions, assembling and testing.
11. Dismantling of Mixer Grinder, identifying the parts, checking the conditions, assembling and testing.
12. Dismantling of Wet Grinder, identifying the parts, checking the conditions, assembling and testing.
13. Assembling the accessories of ceiling fan and energy efficient fan, test the connections of winding & capacitor and run the fan with speed regulator.
14. Dismantling of induction heater, identifying the parts, checking the conditions, assembling and testing.
15. Assembling and testing an LED bulb.

PART C

16. Study of Arduino based IOT **(Not for Examination)**

LIST OF EQUIPMENTS

S. No.	Equipment Name	Quantity
1.	Arduino UNO Board	10
2	LED Module	5
3	Relay Module	2
4	RGB LED	20
5	220 ohm resistors (0.5 watt)	1 Packet
6	LDR	10
7	Motor Driver	5
8	DC gear motor (Arduino compatible)	5
9	Servo motor (Arduino compatible)	5
10	Ultrasonic sensor module	5
11	Moisture Sensor Module	5
12	IR Sensor Module	5
13	Push Button Module	5
14	Buzzer	5
15	Robot Chassis with motors and wheels	5
16	Tools: Screw driver, Cutting pliers, Wire Stripper, Hammer, Spanner set, Line Tester, Nose pliers.	Each 2 set
17	Personal Protective Equipments: Safety helmet, Google, Safety gloves, Nose mask, Ear plug, Safety Belt.	Each 2 set
18	Automatic Iron Box	2
19	Wet Grinder	2
20	Mixer Grinder	2
21	Ceiling Fan, Energy efficient fan	2 each
22	LED Light, PCB, Driver Circuit and Outer Cover	10
23	Induction Heater	1
24	16X2 LCD Display	5
25	Breadboard	10
26	Jumper wires(M-M,M-F,F-F)	3 sets

Detailed Allocation of Marks for External Assessment

Scheme of valuation in TEE		
1.	CIRCUIT DIAGRAM/PROGRAM	30
2.	CONNECTION/EXECUTION	20
3.	OUTPUT	20
4.	VIVA VOCE	05
	Total	**75**

VIRUDHUNAGAR S.VELLAICHAMY NADAR POLYTECHNIC COLLEGE (AUTONOMOUS)

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VIRUDHUNAGAR – 626 001

N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC304

Term : V

Course Name : ADVANCED COMMUNICATION SYSTEMS

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
Advanced Communication Systems	Hours / Week	Hours / Term	Marks			Duration
	6	90	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Hours
1.	RADAR AND NAVIGATIONAL AIDS, TELEPHONY & FAX	18
2.	OPTICAL COMMUNICATION	18
3.	SATELLITE & MICROWAVE COMMUNICATION	18
4.	MOBILE COMMUNICATION	18
5.	TELEVISION SYSTEMS & CCTV	18
	Total	90

Course Outcomes:

On successful completion of the course, the student will be able to:

C304.1	Explain the working principles of RADAR, Electronics Exchange and facsimile communication.
C304.2	Describe the fundamental of Optical communication and Optical sources, Optical detectors.
C304.3	Discuss about the fundamentals of Satellite and Microwave Communication.
C304.4	Comprehend about digital cellular system – GSM.
C304.5	Describe about the Describe about the Television Systems & CCTV

Course Outcome linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Teaching Hrs.
C304.1	Explain the working principles of RADAR, Electronics Exchange and facsimile communication.	***R/U/A***	1,2,5	18
C304.2	Describe the fundamental of Optical communication and Optical sources, Optical detectors.	***R/U/A***	2,5,7	18
C304.3	Discuss about the fundamentals of Satellite and Microwave Communication.	***R/U/A***	2,5,7	18
C304.4	Comprehend about digital cellular system – GSM.	***R/U/A***	2,5	18
C304.5	Describe about the Television Systems & CCTV.	***R/U/A***	2,4,5	18
		Total sessions		90

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	Explain the working principles of RADAR, Electronics Exchange and facsimile communication	18	25	**2**	**18**	**5**	17.86
II	Describe the fundamental of Optical communication and Optical sources, Optical detectors	18	25	**2**	**18**	**5**	17.86
III	Discuss about the fundamentals of Satellite and Microwave Communication	18	25	**2**	**18**	**5**	17.86
IV	Comprehend about digital cellular system – GSM	18	25	**2**	**18**	**5**	17.86
V	Describe about the Television Systems & CCTV	18	25	**2**	**18**	**5**	17.86
I to V *****			**15**	**6**	**9**	**0**	**10.70**
	Total	**90**	**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
Advanced Communication Systems	**1**	**3**	**--**	**1**	**3**	**--**	**2**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**RADAR AND NAVIGATIONAL AIDS, TELEPHONY &FAX** **Radar and Navigational Aids:** Basic Radar System– Applications – Radar Range Equation (Qualitative Treatment Only) – Factors Influencing Maximum Range – Basic Pulsed Radar System – Block Diagram – Display Methods- A - Scope, PPI Display - Instrument Landing System – Ground Controlled Approach System. **Telephony system:** Telephone System–Public Switched Telephone Network (PSTN) - Electronic Switching System – Block Diagram – ISDN – Architecture, Features- Video Phone – Block Diagram. **Facsimile Communication System(FAX):** Facsimile Sender- Cylindrical Scanning – Facsimile Receiver- Synchronization – Phasing - Index Of Cooperation (IOC) – Direct Recording.	**18**
II	**OPTICAL COMMUNICATION:** **Fundamental of Optical Communication System:** Block diagram – advantages of optical fiber Communication systems – principles of light transmission in a fiber using Ray Theory – Single mode fibers, multimode fibers – step index fibers, graded index fibers (basic concepts only). **Attenuation in Optical Fibers:** Absorption losses, scattering losses, bending losses, core and cladding losses. **Optical Sources:** LED - semiconductor LASER – Principles. **Optical Detectors:** PIN and APD diodes –Connectors - Splices – Couplers-Optical transmitter – Block diagram – optical receiver - Block diagram. **Application of Optical Fibers**: Networking, Industry, FTTH and Military.	**18**
III	**SATELLITE & MICROWAVE COMMUNICATION** **Satellite system:** Kepler's I,II,III laws – orbits – types- Geostationary synchronous satellites- Advantages – Apogee -Perigee- Active and passive satellite – Earth eclipse of satellite **Antenna:** Parabolic reflector antenna – cassegrain antenna. **Space Segment:** Power supply- Altitude control- station keeping – Transponders – TT and C subsystem – Thermal control – Antenna subsystem. **Earth Segment:** Block diagram of Transmit-receive earth station- Satellite mobile services- Basics of GPS- Block diagram of receive only dish TV system. **Microwave Communication**: Microwave frequency ranges - microwave devices – Parametric amplifiers –Travelling wave tubes – simple block diagram of microwave transmitter, receiver and microwave link repeater.	**18**

IV	**MOBILE COMMUNICATION: (Qualitative Treatment only)** **Cellular Telephone:** Evolution of mobile communication - comparison of 2G, 3G, 4G and 5G. Fundamental concepts – Simplified Cellular telephone system - frequency reuse – Interference – Co - Channel Interference – Adjacent Channel Interference – Improving coverage and capacity in cellular systems - cell splitting – sectoring - Roaming and Handoff. **Digital Cellular System:** Global system for mobile communications (GSM) –GSM services - GSM System Architecture – Basics of GPRS and EDGE, IoT-Definition and characteristics of IoT- An IoT architecture outline.	**18**
V	**TELEVISION SYSTEMS & CCTV:** **Monochrome** & **Color Television:** Scanning principles - synchronization - aspect ratio- composite video signal- TV broadcasting standards - Basic block diagram of Monochrome TV transmitter - TV receiver. **Color TV**: Principles of color transmission and reception- color CCD camera. PAL color TV receiver – digital colour TV receiver - various digital TV broadcasting standards - LCD, LED display unit - Plasma display- cable TV, IPTV. **CCTV:** CCTV working- Different types of cameras – Conventional camera, Infra-Red (IR) camera, Thermal camera and IP based camera- Digital video recorder - CCTV for surveillance.	**18**

Text Book:

1.Electronic communication systems - Kennedy - Davis -Fourth Edition - Tata McGraw Hill -
1999.
2.Electronics communication - Dennis Roddy and John coolen - Third Edition - PHI – 1988.
3.Modern Television Practice – Transmission, Reception, Applications R.R.Gulati New age
international 5th Edition 2015

Reference Book:

1.Optical fiber communication - Gerd Keiser - Third Edition - McGraw Hill – 2000.
2. Satellite communication - Dr. D.C. Agarwal - Third Edition - Khanna publishers – 1995.

3. Electronic Communications systems - Fundamentals through Advanced - Wayne Tomasi
Fifth Edition - Pearson Education – 2005.
4. Mobile Communications-Jochen Schiller – Second Edition-Pearson Education.

MODEL QUESTION PAPER – I

Term : V Time : 3Hrs

Programme : Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : Advanced Communication Systems Code : N1EC304

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. What are the applications of RADAR?
2. Give short notes on GPS?
3. Define GSM.
4. Define IOC.
5. What is a parametric amplifier?
6. What is FDMA?
7. What is flicker?
8. What is Aspect ratio?

PART – B

9. Write a note on ISDN.
10. Give some applications and advantages of optical fiber.
11. What is apogee & perigee?
12. Write notes on EDGE.
13. What are microwave devices?
14. What are the advantages of satellite communication system?
15. What is CCTV?
16. Mention the services of GSM.

[Turn over …..

PART – C

17. (a) Explain the operation of pulsed RADAR system.

(Or)

(b) Draw and explain the architecture of ISDN system.

18. (a) Draw and explain the principal components of optical communication

(Or)

(b) Explain the any two applications of Fiber optic communication.

19. (a) Draw and explain the Satellite Space Segment Sub-systems.

(Or)

(b) Explain the Transmit-Receive earth station.

20. (a) Explain GSM system architecture with neat diagram.

(Or)

(b) How to improve the coverage and capacity in Cellular systems?

21. (a) Explain the PAL Color TV receiver with block diagram.

(Or)

(b) Explain the LCD and LED Television.

MODEL QUESTION PAPER – II

Term : V Time : 3Hrs

Programme : Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : Advanced Communication Systems Code : N1EC304

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. What is ILS?
2. What is PSTN?
3. Give example for Optical Source.
4. Mention one advantage of Optical Fiber.
5. What is Perigee?
6. What is Roaming?
7. List out the Camera Tubes?
8. What is interlaced scanning?

PART – B

9. Define IOC.
10. What are the two types of semi-conductor LASER?
11. Give one example of Microwave Device.
12. State any two losses in Optical Fiber.
13. What is Hand-off?
14. What is Scanning?
15. What is GPRS?
16. What are the display methods of RADAR?

[Turn over …..

PART – C

17. (a) Elaborate the Aircraft Landing System..

(Or)

(b) Detailed notes on Facsimile Sender and Receiver.

18. (a) Explain the various types of losses in optical fibers.

(Or)

(b) Elaborate the Optical Sources.

19. (a) Detailed notes on Parabolic reflector Antenna with neat diagrams.

(Or)

(b) Draw and Explain the Microwave Link Repeater.

20. (a) Detailed notes on Frequency reuse and Interference.

(Or)

(b) Explain the Satellite Multiple Access Techniques.

21. (a) Draw and explain the Monochrome TV transmitter and Receiver.
.

(Or)

(b) Explain the different types of CCTV cameras with neat diagrams.

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N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC305

Term : V

Course Name : MICRO CONTROLLER

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
MICRO CONTROLLER	Hours / Week	Hours / Term	Marks			Duration
	6	90	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Hours
1.	ARCHITECTURE & INSTRUCTION SET OF 8051	20
2.	PROGRAMMING EXAMPLES	18
3.	TIMER, INTERRUPT AND SERIAL COMMUNICATION	18
4.	INTERFACING TECHNIQUES	18
5.	INTRODUCTION TO ANDROID	16
	Total	90

Course Outcomes:

On successful completion of the course, the student will be able to:

C305.1	Understand the architecture and instruction set of 8051 Microcontroller.
C305.2	Understand the various addressing modes and Write assembly language program to implement arithmetic and logic operations for 8051 Microcontroller.
C305.3	Comprehend interrupt structure, timer and serial data communication.
C305.4	Interface peripheral devices with 8051 microcontroller.
C305.5	Understand the concepts of Android operating system.

Course Outcome linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		**CL**	**Linked PO**	**Teaching Hrs.**
C305.1	Understand the architecture and instruction set of 8051 Microcontroller	***R/U/A***	1	20
C305.2	Understand the various addressing modes and Write assembly language program to implement arithmetic and logic operations for 8051 Microcontroller	***R/U/A***	1,2	18
C305.3	Comprehend interrupt structure, timer and serial data communication	***R/U/A***	1,2,3	18
C305.4	Interface peripheral devices with 8051 microcontroller	***R/U/A***	1,2,3	18
C305.5	Understand the concepts of Android operating system	***R/U/A***	1,5,7	16
		Total sessions		90

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	ARCHITECTURE & INSTRUCTION SET OF 8051	20	25	2	18	5	17.86
II	PROGRAMMING EXAMPLES	18	25	2	18	5	17.86
III	TIMER, INTERRUPT AND SERIAL COMMUNICATION	18	25	2	18	5	17.86
IV	INTERFACING TECHNIQUES	18	25	2	18	5	17.86
V	INTRODUCTION TO ANDROID	16	25	2	18	5	17.86
I to V *			15	**6**	**9**	**0**	10.70
	Total	90	**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
MICRO CONTROLLER	**3**	**3**	**2**	**-**	**1**	**-**	**1**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**ARCHITECTURE & INSTRUCTION SET OF 8051:** **1.1 ARCHITECTURE OF 8051** Comparison of Microprocessor and Microcontroller – Block diagram of Microcontroller –Functions of each block – Pin details of 8051 – ALU –ROM– RAM – Memory Organization of 8051 – Special Function Registers –Program Counter – PSW register –Stack – I/O Ports – Interrupt –Serial Port – Oscillator and Clock – Clock Cycle – State Machine Cycle –Instruction cycle – Reset – Power on Reset –Overview of 8051 family. **1.2 INSTRUCTION SET OF 8051** Instruction set of 8051 – Classification of 8051 Instructions – Data transfer instructions – Arithmetic Instructions – Logical instructions – Branching instructions – Bit Manipulation Instructions.	20
II	**PROGRAMMING EXAMPLE** **2.1 ASSEMBLER AND ADDRESSING MODES** Assembling and running an 8051 program –Structure of Assembly Language –Assembler directives –Addressing modes of 8051. **2.2 PROGRAMS** Multi byte Addition – 8 Bit Multiplication and Division – Biggest Number / Smallest Number – Ascending order / Descending order – BCD to ASCII Conversion – ASCII to Binary Conversion –Odd Parity Generator – Even Parity Generator –Time delay Routines.	18
III	**TIMER, INTERRUPT AND SERIAL COMMUNICATION** **3.1 TIMER** Programming 8051 Timers – Timer 0 and Timer 1 registers – Mode 1 Programming – Mode 2 Programming. **3.2 INTERRUPT** 8051 Interrupts – Programming Timer Interrupts – Programming external hardware interrupts – Programming the serial communication interrupt –Interrupt priority in 8051. **3.3 SERIAL COMMUNICATION** Basics of Serial programming – RS 232 Standards – 8051connection to RS 232 – 8051 Serial Communication Programming – Programming 8051 to transmit data serially – Programming 8051 to Receive data serially.	18

IV	**INTERFACING TECHNIQUES** Interfacing external memory to 8051– IC 8255 – block diagram – modes of 8255 – 8051 interfacing with the8255 – ASM Programming – Sensor interfacing – ADC interfacing – DAC interfacing – Keyboard interfacing – Seven segment LED Display Interfacing – Stepper Motor interfacing –DC motor interfacing using PWM.	18
V	**INTRODUCTION TO ANDROID** Introduction – History – Features and Android Architecture – Android Environment Setup – SDK – Android Application components – Intents – Broadcast receivers, Services – Android as a sensor – Comparison of Android OS & iOS.	16

Text Book:

1. Microcontrollers, Principles and Applications- Ajit pal- PHI Ltd.,
2. 8051 Microcontroller and Embedded Systems using Assembly and C- Mazidi,Mazidi and
   D.MacKinlay- Pearson Education, Low Price Edition.

Reference Book:

1. Microprocessor and Microcontroller- R.Theagarajan- SciTechPublication, Chennai.
2. 8051Micro controller - Kenneth Ayala - Thomas India Edition.
3. Android (Operating Systems)- Aaron Bryan.

MODEL QUESTION PAPER – I

Term	:	V	Time	: 3 Hrs
Programme	:	Diploma in Electronics and Communication Engineering	Max. Marks : 75	
Course	:	Microcontroller	Code : N1EC305	

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define ALU.
2. What is an assembler?
3. What is meant by interrupt?
4. What is the use of RS232C standard?
5. What are the modes of 8255?
6. Define PWM.
7. Name few sensors available in mobile phones.
8. List out types of Assembler directives.

PART – B

9. Write about PSW register.
10. Write an ALP for 8 bit multiplication.
11. What are the functions of TF0 and TR0 bits in TCON register?
12. Explain Interrupt priority in 8051.
13. Write the control word format of 8255.
14. Draw the interfacing diagram of ADC.
15. What are the features of Android OS?
16. Compare Android OS and iOS.

[Turn over …..

PART – C

17. (a) Draw and explain the Architecture of 8051 Microcontroller.

(Or)

(b) Draw and explain the memory organization of 8051 Microcontroller.

18. (a) Explain the different types of addressing modes used in 8051.

(Or)

(b) Write an ALP for Mulitibyte addition.

19. (a) Explain the programming of 8051 to transmit / receive data serially.

(Or)

(b) Explain TMOD and TCON Registers.

20. (a) Draw and explain the block diagram of 8255 PPI IC.

(Or)

(b) Draw and explain the operation of stepper motor interfacing.

21. (a) With neat diagram explain the architecture of android OS.

(Or)

(b) Explain Android environment setup.

MODEL QUESTION PAPER - II

Term	:	V	Time	: 3 Hrs
Programme	:	Diploma in Electronics and Communication Engineering	Max. Marks	: 75
Course	:	Microcontroller	Code	: N1EC305

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define ALE.
2. Write any two Data transfer instruction in 8051 Microcontroller.
3. What is an assembler?
4. What is the function of TXD and RXD pins in 8051 MC?
5. State the function of M1 and M0 bits in TMOD register.
6. What is signal conditioning?
7. Write down any two features of Android OS.
8. Write the structure of assembly language program.

PART – B

9. Compare Microprocessor and Microcontroller.
10. Explain program counter.
11. Write a simple ALP to divide two numbers.
12. Explain TCON register.
13. Draw the interfacing diagram of DC motor with 8051 MC.
14. Explain about control word register in 8255.
15. Name any five Android versions.
16. Draw the diagram of RS232 interface with 8051 MC.

[Turn over …..

PART – C

17. (a) Draw and explain the pin diagram of 8051 Microcontroller .

(Or)

(b) Classify the 8051 instructions based on their functions. Explain them with example.

18. (a) Explain the different types of addressing modes used in 8051 MC.

(Or)

(b) Write an ALP for to find the largest number in an array.

19. (a) Explain Mode 1 and Mode 2 timer programming.

(Or)

(b) Explain IE and IP Registers.

20. (a) Explain external memory interfacing with 8051 MC.

(Or)

(b) Explain DC motor interfacing with PWM.

21. (a) Explain Android Application Components.

(Or)

(b) Compare Android OS & iOS.

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(Affiliated to Directorate of Technical Education, Chennai-25)

VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme : Diploma in Electronics & Communication Engineering

Course code : N1EC306

Term : V

Course Name : VERY LARGE SCALE INTEGRATION

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
Very Large Scale Integration	Hours / Week	Hours / Term	Marks			Duration
	6	90	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Time in Hrs
1.	Combinational Logic Circuit design	18
2.	VHDL for Combinational Circuits	18
3.	Sequential Circuit design	18
4.	VHDL for Sequential Circuit	18
5.	ASICs, PLDs AND FPGA	18
	Total	90

Course Outcomes:

On successful completion of the course, the student will be able to:

C306.1	Understand the usage of MOSFET in IC.
C306.2	Develop VHDL code for combinational circuits.
C306.3	Develop VHDL code for sequential circuits.
C306.4	Develop VHDL code for Flipflops and counters.
C306.5	Know about types of ASIC and FPGA structure.

Course Outcome linkage to Cognitive Level

Course Outcome		CL	Linked PO	Linked PSO	Teaching Hrs
C306.1	Understand the application of MOSFET in IC.	***R/U/A***	1,2	1,2	18
C306.2	Develop the VHDL code for combinational circuits.	***R/U/A***	1,2,4	2	18
C306.3	Develop the own VHDL code for sequential circuits.	***R/U/A***	1,2,4,5	2	18
C306.4	Write own VHDL code for Flipflops and counters.	***R/U/A***	1,2,4,7	2	18
C306.5	Know about types of ASIC and FPGA structure	***R/U/A***	1,7	2	18
		Total sessions			**90**

Legends : R- Remember, U- Understand, A- Application

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hour	Max. Marks per Unit	Questions to be set for			Marks weightage (%)
				R	U	A	
I	Combinational Logic Circuit	18	25	**2**	**18**	**5**	17.86
II	VHDL For Combinational Logic Circuit	18	25	**2**	**18**	**5**	17.86
III	Sequential Logic Circuit	18	25	**2**	**18**	**5**	17.86
IV	VHDL For Sequential Logic Circuit	18	25	**2**	**18**	**5**	17.86
V	PLD And FPGA Circuits	18	25	**2**	**18**	**5**	17.86
I to V*			15	**6**	**9**	**0**	10.70
	Total	90	**140**	**16**	**99**	**25**	**100**

***3 x 2 Marks and 3 x3 Marks from any unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
VERY LARGE SCALE INTEGRATION	**3**	**3**		**3**	**2**		**3**

Course-PSO Attainment Matrix:

Course	Programme Specific Outcomes	
	1	2
VERY LARGE SCALE INTEGRATION	**1**	**3**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

VERY LARGE SCALE INTEGRATION

DETAILED SYLLABUS

Contents : Theory

Unit	Name of the Topic	Hours
I	**1.1 COMBINATIONAL LOGIC CIRCUIT DESIGN:** NMOS and CMOS logic implementation of Switch, NOT, AND, OR, NAND, and NOR Gates CMOS Transmission Gate. Digital logic variable, functions, inversion, gate/circuits, Boolean algebra and circuit synthesis using gates (Up to 4 variables). **1.2 COMBINATIONAL CIRCUIT BUILDING BLOCKS**: Circuit synthesis using Multiplexer(Shanon's Theorm), Demultiplexer, Encoders and Decoders, Arithmetic adder, Subtractor and Comparator circuits, Look up tables (LUT) for 2 variables , Hazards and races.	18
II	**2.1 VHDL FOR COMBINATIONAL CIRCUITS**: Introduction to VLSI and its design process.(Definitions only for Design entry through Schematics and HDL, Logic Sythesis, Pre-Layout Simulation, System Partitioning, Floor Planning, Placement, Routing, Circuit Extraction and Post Layout Simulation) Introduction to CAD tools. Introduction to HDL and different level of abstractions. VHDL Statements and Assignments. **2.2 VHDL CODE:** Implementation of AND, OR, NAND, NOR gates, Mux, Demux, Encoder, decoder. Four bit Arithmetic adder, sub tractor and comparator in VHDL.	18
III	**3.1 SEQUENTIAL CIRCUIT DESIGN**: Introduction/Refreshing to Flip- flops and its excitation table, counters and Shift registers, Setup time, Hold Time, Propogation delay, Maximum permissible clock frequency in a D flip Flop. **DESIGN STEPS:** State diagram, State table, state assignment. Example for moore and mealy machines. Design of modulo counter (upto 3 bit) with only D flip-flops through state diagram.	18
IV	**4.1 VHDL FOR SEQUENTIAL CIRCUIT:** VHDL constructs for storage elements. VHDL code for D Latch / D, JK and T Flip-flops with or without reset input. **VHDL EXAMPLES**: Counters: Synchronous counters-2 bit &3 bit up counter. 3 bit up/down counter, Decade counter, Johnson Counter, VHDL code for Test Bench for 3 bit ripple counter.	18

V	**ASICs, PLDs AND FPGA**: **ASICs :** Standard IC Vs Custom IC – ASIC – Types of ASICs (Full Custom, Semi Custom & Programmale ASICs – only definitions). **PLD :** Introduction to PROM,PLA and PAL. Implementation of combinational circuits with PROM, PAL and PLA (up to 4 variables). Comparison between PROM, PAL and PLA. **FPGA :** Introduction to Complex Programmable Logic device, Field Programmable Gate Array - Functional diagram of ACT1 Logic module, XC 3000 Combinational Logic Block. **Programmable Interconnects:** Antifuse, SRAM and EEPROM.	18

Text Book:

1. Digital Design" M.Morris Mano Michael D Ciletti Pearson Education 2008.

2. "Fundamentals of Digital Logic with VHDL design" Stephen brown and Vranesic 2nd edition .

3. "VHDL Primer" Bhasker J Prentice Hall India -2009 -

Reference Book:

1. "Digital Electronics with PLD Integration" Nigel P. Cook, Prentice Hall, 2000.

2. "Programmable Logic Handbook: PLD, CPLD, and FPGA" Ashok K.Sharma, Mcgraw-Hill, 1998.

3. "Digital Logic Simulation and CPLD Programming with VHDL" Steve Waterman Prentice Hall.

MODEL QUESTION PAPER – I

Term : V Time : 3 Hours

Programme : Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : Very Large Scale Integration Code : N1EC306

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Draw the transistor level implementation of NAND gate.
2. Draw CMOS inverter.
3. State the difference between schematics and HDL.
4. What do you mean by Pre-Layout Simulation.
5. Write the Excitation table for a D Flip Flop.
6. What do you mean by set-up-time?
7. Write VHDL Code for D flip flop.
8. What do you mean by PLA?

PART – B

9. Briefly explain the CMOS transmission gate operation.
10. Draw a circuit using 2 input LUT for the function f= x1.x2 + x1.x2.
11. Develop VHDL code for implementing decoder.
12. How will you calculate maximum permissible clock frequency in D Flip Flop.
13. State the differences between Moore & Mealey machines.
14. Develop VHDL code for implementing 'T' Flip Flop.
15. Explain the difference between CPLD and FPGA.
16. Develop VHDL code for 2 input MUX.

[Turn over …..

PART – C

17. (a) Implement the function F = Σ 1,2,3,5.7,10,13 with minimal gates.

(Or)

(b) Using Shanon's theorem, implement the function f = w1w3 +w1w2+w1w3 using 2:1 mux.

18. (a) Explain VLSI Design flow with flowchart.

(Or)

(b) Draw the block diagram of four-bit-Arithmetic Adder and develop the VHDL code for the same.

19. (a) Explain the state diagram, state table , state assignment for a MOORE machine.

(Or)

(b) Design a modulo 5 counter using D flip flop. Use proper excitation table and state diagram.

20. (a) Develop VHDL code for implementing modulo 6 UP / DOWN counter (Note : Separate Up or Down mode selection has to be given)

(Or)

(b) Develop VHDL code for test bench for 3 bit ripple counter.

21. (a) Explain the functional block diagram of ACTEL ACT1 Logic module.

(Or)

(b) Explain the Static RAM and EEPROM.

MODEL QUESTION PAPER – II

Term : V Time: 3 Hours

Programme : Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : Very Large Scale Integration Code : N1EC306

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Draw the CMOS OR gate circuit.
2. Why CMOS is better than NMOS and PMOS in realization of gates?
3. Define Simulation.
4. What are the types of generating statement?
5. What is a state table?
6. State the types of shift registers used in digital circuits.
7. Define storage elements and give examples.
8. What is an antifuse?

PART –B

9. Draw the CMOS transmission gate.
10. Implement AND gate using LUT.
11. List down the different levels of abstraction in HDL.
12. Draw the excitation table of JK Flip Flop.
13. State the differences between Mealy and Moore Machine.
14. Write the VHDL code for D Latch.
15. State the differences between Full Custom and Semi Custom ASIC.
16. Draw the general structure of CPLD.

[Turn over …..

PART – C

17. (a) Implement the function F = Σ 1,2,3,5.7,10,13 with minimal gates.

(Or)

(b) Draw the Arithmetic Adder and Subtractor.

18. (a) Explain VLSI Design flow with flowchart.

(Or)

(b)Write the VHDL Code for Decoder and Comparator.

19. (a) Design a modulo 4 counter from State diagram using D Flip Flop.

(Or)

(b) Design a modulo 7 counter using D flip flop. Use proper excitation table and state diagram.

20. (a) Develop VHDL code for implementing T Flip Flop with and without reset.

(Or)

(b) Develop VHDL code for Serial Adder.

21. (a) Implement the function F = Σ 1,3,5,7,13 using PLA and PAL.

(Or)

(b) Explain XC 3000 Combinational Logic Block of Xilinx FPGA.

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N1 - SCHEME

(Implements from the Academic year 2019-2020 onwards)

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC403

Term : V

Course Name : ELECTIVE THEORY – I
1. DIGITAL COMMUNICATION

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
ELECTIVE THEORY – I 1. DIGITAL COMMUNICATION	Hours / Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Hours
1	ANALOG TO DIGITAL MODULATION	15
2	DIGITAL TRANSMISSION	15
3	SPREAD SPECTRUM &MULTIPLE ACCESS TECHNIQUES.	15
4	DATA, SPEECH AND VIDEO COMPRESSION.	15
5	WIRELESS NETWORKS & CRYPTOGRAPHY	15
	Total	75

Course Outcomes:

On successful completion of the course, the student will be able to:

C403.1	Understand the basics of digital communication and data transmission modes**.**
C403.2	Analyze different types of line coding and digital modulation techniques.
C403.3	Understand and analyze the concepts of multiplexing, multiple access techniques.
C403.4	Distinguish different types of source coding methods and compression techniques.
C403.5	Understand and analyze the concepts of Wireless Networks and cryptography

Course Outcome linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Linked PSO	Teaching Hrs
C403.1	Understand the basics of digital communication and data transmission modes**.**	**R/U/A**	1,3	1	15
C403.2	Analyze different types of line coding and digital modulation techniques.	**R/U/A**	1,3,5	1	15
C403.3	Understand and analyze the concepts of multiple access and spread spectrum techniques.	**R/U/A**	1,2,3	1	15
C403.4	Distinguish different types of source coding methods and compression techniques.	**R/U/A**	1,2,3,7	1	15
C403.5	Understand and analyze the concepts of wireless networks and cryptography	**R/U/A**	1,5,6,7	1	15
		Total sessions			75

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hour	Max. Marks per Unit	Questions to be set for			Marks weightage (%)
				R	U	A	
I	ANALOG TO DIGITAL MODULATION	15	25	***2***	***18***	***5***	*17.86*
II	DIGITAL TRANSMISSION	15	25	***2***	***18***	***5***	*17.86*
III	SPREAD SPECTRUM &MULTIPLE ACCESS TECHNIQUES.	15	25	***2***	***18***	***5***	*17.86*
IV	DATA, SPEECH AND VIDEO COMPRESSION.	15	25	***2***	***18***	***5***	*17.86*
V	WIRELESS NETWORKS & CRYPTOGRAPHY	15	25	***2***	***18***	***5***	*17.86*
I to V			15	***6***	***9***	***0***	*10.70*
	Total	75	**140**	**16**	**99**	**25**	**100**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
DIGITAL COMMUNICATION	**3**	**1**	**3**	**-**	**1**	**-**	**1**

Course-PSO Attainment Matrix

Course	Programme Specific Outcomes	
	1	2
DIGITAL COMMUNICATION	**3**	**-**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**ANALOG TO DIGITAL MODULATION** **ANALOG AND DIGITAL SIGNALS: A**dvantages of digital communication over analog communication -block diagram of digital communication system. **PCM:** Block diagram-sampling-quantization- uniform and non uniform quantization - Companding – regeneration. **DELTA MODULATION AND DEMODULATION:** Block diagram-advantages and disadvantages-DPCM-adaptive DPCM. **DATA TRANSMISSION MODES**: Serial and parallel transmission-synchronous and asynchronous transmission.	**15**
II	**DIGITAL TRANSMISSION** **TRANSMISSION OF DIGITAL SIGNALS**: Baseband transmission – low pass channel-broadband transmission- band pass channel-Transmission impairments-attenuation-distortion-noise- Nyquist bit rate-Shannon limit on information capacity. **DIGITAL TO DIGITAL CONVERSION**: Line coding-unipolar-polar-NRZ-L,NRZ-I, RZ, Manchester, differential Manchester- bipolar-AMI, Pseudoternary and block coding. **DIGITAL TO ANALOG MODULATION**:ASK, FSK, PSK (definition, waveforms and comparison) - Advanced FSK technique-GMSK-Advanced PSK Technique-BPSK,QPSK-QAM.	**15**
III	**SPREAD SPECTRUM &MULTIPLE ACCESS TECHNIQUES** **MULTIPLEXING:** SDM-FDM-TDM- synchronous TDM-T-1 lines and frames, statistical TDM, CDM. **SPREAD SPECTRUM TECHNIQUE**: DSSS, FHSS-slow hopping, fast hopping. **MULTIPLE ACCESS**: Frequency division multiple access, Time division multiple access, Code division multiple access.	**15**
IV	**DATA, SPEECH AND VIDEO COMPRESSION** **CODING :** Shannon-Fano algorithm, Huffman code - Adaptive Huffman coding – Escape code – Overflow. **DICTIONARY BASED COMPRESSION:** LZW Coding. **DIGITAL AUDIO CONCEPTS:** Fundamental – Sampling variables – PC based lossless compression of sound – Lossy compression – Silence compression. **VIDEO COMPRESSION STANDARDS**: MPEG, JPEG.	**15**

V	**WIRELESS NETWORKS & CRYPTOGRAPHY** **INTRODUCTION**: Difference between wired and wireless LAN- Evolution of wireless networks 1G, 2G, 3G, 4G and5G. **WLAN:** WLAN Architecture, MAC control in WLAN, CSMA/CA protocol with flowchart-FHSS-DSSS Techniques in WLAN- Comparison of features of wireless standards. 802.11 a,b,g,h,i,p. **WPAN:** Bluetooth – Piconet – Scatternet - Features – Zigbee, Z-wave – 802.16 standards comparison. Wi-Fi and Wi max, Architecture. **CRYPTOGRAPHY:** Encryption and decryption –symmetric key cryptography-substitution cipher - monoalphabetic - polyalphabetic - asymmetric key cryptography.	**15**

Text Book:

1. Data Communications and Networking – Behrouz A Forouzan- TMH-4th Edition
2. Mobile Communications-Jochen Schiller-Pearson Education- Second Edition.

Reference Book:

1. Digital communication – Simon Haykins – Wiley India Edition.
2. Digital communication – P. Ramakrishna Rao – TMH.
3. Introduction to Digital Communication System by NIIT, PHI Learning Private Ltd, New Delhi.
4. Principles of communication systems By Taub & Schilling- TMH- Third Edition.
5. Principles of Digital communication – J.S. Chitode – Tech. Publications – Pune.
6. Wireless Communications –Theodore S. Rappaport- PHI- Second Edition.

MODEL QUESTION PAPER – I

Term : V Time : 3 Hours

Programme : Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : Elective Theory – I
1. Digital Communication Course Code: N1EC403

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Give any two advantages of digital communication over analog communication.
2. Define quantization.
3. Expand AMI.
4. What are the two types of TDM?
5. Expand DSSS?
6. What is the advantage of Adaptive Huffman coding over Huffman coding?
7. Define piconet.
8. Write the expression for Shannon limit on information capacity.

PART – B

9. What is quantization noise? How it can be reduced?
10. Compare baseband and broadband transmission.
11. Write notes on QAM.
12. Compare slow hopping and fast hopping.
13. Explain Silence compression.
14. Write short notes on digital audio concepts.
15. Write short notes on Asymmetric key cryptography.
16. Compare 802.11 wireless standards.

[Turn over …..

PART – C

17. (a) Draw the block diagram of digital communication system and explain.

(Or)

(b) Draw the block diagram of PCM transmitter and receiver and explain each block.

18. (a) Explain (i) NRZ-L (ii) NRZ-I (iii) Manchester coding.

(Or)

(b) Explain (i) GMSK (ii) QPSK with neat diagrams.

19. (a) Explain Frequency Hopping Spread spectrum technique with neat diagram.

(Or)

(b) Explain various multiplexing techniques with neat diagram.

20. (a) Write the algorithm of Shannon fano encoding. Explain with an example.

(Or)

(b) Explain MPEG video compression standard with neat diagram.

21. (a) Explain with neat diagram, the system architecture of infrastructure based WLAN and ad-hoc wireless LAN.

(Or)

(b) Explain CSMA / CA – medium access control technique used in WLAN with neat flow chart.

MODEL QUESTION PAPER – II

Term : V Time : 3 Hours

Programme : Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : Elective Theory – I
1. Digital Communication Course Code: N1EC403

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. What is sampling?
2. Define DPCM.
3. Name any two polar coding schemes.
4. Compare baseband and broadband transmission.
5. What is multiplexing in communication?
6. Where is the need for Spread Spectrum Technique?
7. What is lossy compression?
8. Name the protocol used for medium access in WLAN

PART – B

9. Compare Serial and Parallel Transmission.
10. Write short notes on Companding.
11. What are transmission impairments?
12. Explain Manchester coding with neat diagram.
13. Write short notes on CDMA
14. Write short notes on Dictionary based compression.
15. Give the advantages of WLAN.
16. Write short notes on Zigbee communication.

[Turn over …..

PART – C

17. (a) Draw the block diagram for Delta Modulator and Demodulator and explain.

(Or)

(b) Explain different data transmission modes in detail with neat diagrams

18. (a) Explain block coding with example.

.

(Or)

(b) Explain advance PSK technique QPSK with necessary diagram.

19. (a) Explain Time Division Multiplexing and its types with neat diagrams

(Or)

(b) Explain DSSS technique with neat diagram.

20. (a) Write the algorithm of Huffman encoding. Explain with an example.

(Or)

(b) Explain JPEG video compression standard with neat diagram.

21. (a) Give the features of Bluetooth network. Explain Pico net and Scatter net, with neat diagrams.

(Or)

(b) Write short notes on Symmetry Key and Asymmetry Key Cryptography with diagram.

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N1 - SCHEME

(Implements from the Academic year 2019-2020 onwards)

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC404

Term : V

Course Name : ELECTIVE THEORY – I
2. Mobile Communication

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
ELECTIVE THEORY – I 2.Mobile Communication	Hours / Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Hours
1	Introduction to Mobile Communication	**15**
2	Broadcast Systems	15
3	Wireless Transmission (2G)	15
4	Wireless Networking (3G)	15
5	Mobile Network Layer & Transport Layer	15
	Total	75

Course Outcomes:

On successful completion of the course, the student will be able to:

C404.1	Describe the various generations of mobile communication.
C404.2	Understand about the digital broadcasting systems.
C404.3	Understand the services and features of 2nd generation GSM and CDMA(IS-95).
C404.4	Demonstrate the Mobile services of 2.5G-GPRS, WAP and 3G-WCDMA.
C404.5	Explain the functionalities of Mobile Network and Transport Layers.

Course Outcome linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Teaching Hrs
C404.1	Describe the various generations of mobile communication	***R/U/A***	1,3,5	15
C404.2	Understand about the broadcast systems.	***R/U/A***	3,5	15
C404.3	Understand the services and features of 2nd generation34083 3 GSM and CDMA(IS-95)	***R/U/A***	1,3,5	15
C404.4	Demonstrate the Mobile services of 2.5G(GPRS , WAP) and 3G(WCDMA)	***R/U/A***	1,3,5	15
C404.5	Explain the functionalities of Mobile Network Layer	***R/U/A***	3,5	15
		Total sessions		75

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hour	Max. Marks per Unit	Questions to be set for			Marks weightage (%)
				R	U	A	
I	Introduction to Mobile	15	25	***2***	***18***	***5***	*17.86*
II	Broadcast Systems	15	25	***2***	***18***	***5***	*17.86*
III	Wireless Transmission (2G)	15	25	***2***	***18***	***5***	*17.86*
IV	Wireless Networking (3G)	15	25	***2***	***18***	***5***	*17.86*
V	Mobile Network Layer & Transport Layer	15	25	***2***	***18***	***5***	*17.86*
I to V			15	***6***	***9***	***0***	*10.70*
	Total	75	**140**	**16**	**99**	**25**	**100**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
MOBILE COMMUNICATION	**2**		**3**	**-**	**3**	**-**	**-**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**INTRODUCTION TO MOBILE COMMUNICATION** **INTRODUCTION TO MOBILE COMMUNICATION** Evolution of Mobile Radio Communication, Mobile Radio Telephony in India and around the world, Examples of Wireless Communication Systems: Paging system, Cordless telephones systems, Cellular telephone Systems, Trends in Cellular Radio and personal Communications **THE CELLULAR CONCEPT:** Frequency reuse, Channel Assignment strategies, Hand off Strategies, Prioritizing Handoffs, Interference and system capacity, Improving coverage and capacity in cellular systems ,Cell splitting ,Sectoring, Repeaters for range extension	15
II	**BROADCAST SYSTEMS** Introduction – Cyclical repetition of data – Digital audio broadcasting – multimedia object transfer protocol – Digital video broadcasting – DVB data broadcasting, DVB for high speed internet access – Convergence of broadcasting and mobile communications.	15
III	**WIRELESS TRANSMISSION (2G)** Global system for mobile (GSM) - services and features – Architecture -Radio subsystem - channel types - Example of a GSM call - Frame structure for GSM – DECT system architecture, protocol architecture – TETRA – UMTS and IMT-2000 -radio interface, UTRAN, core network, handover CDMA digital cellular standard (IS – 95): Frequency and channel specifications -Forward CDMA channel and Reverse CDMA channel	15
IV	**WIRELESS NETWORKING (3G)** **Mobile Services (2.5G)** **GPRS:** GPRS Functional groups – architecture - network nodes – procedures-billing. **WAP:** WAP Model - WAP Gateway- WAP Protocols - WAP UA prof and caching, wireless bearers for WAP, WAP developer tool kits - Mobile station application execution environment. **Mobile Services (3G):** Paradigm Shifts in 3G Systems - W-CDMA and CDMA 2000 – Improvements on core network - Quality of service in 3G - Wireless OS for 3G handset - 3G systems and field trials - Other trail systems - Impact on manufacture and operator technologies.	15

V	**MOBILE NETWORK LAYER & TRANSPORT LAYER** Mobile IP – Goals, assumptions and requirements, Entities and terminology, IP Packet delivery, Agent discovery, Registration, tunneling and encapsulation, Optimization, Reverse tunneling, IPv6, IP micro- mobility support – Dynamic host configuration protocol – mobile ad-hoc network – routing – destination sequence distance vector – Dynamic source routing – alternative metrics TCP – Congestion control – slow start – fast retransmit/ fast recovery – implications of mobility – Classical TCP improvements – indirect – snooping – Mobile–Transmission timeout freezing – selective retransmission- Transaction oriented – TCP over 2.5/3G wireless networks.	15

Text Book:

1. Mobile Communications - Jochen Schiller - Pearson Education, 2009, Second edition.
2. Wireless Communications Principles and Practice - Theodore S. Rappaport - Pearson Education, 2003.

Reference Book:

1. Wireless and Mobile Network Architectures - Yi-BingLin, Imrich Chlamtac - Wiley, 2001.
2. Mobile Cellular Communication - Gottapu Sasibhushana Rao - Pearson Education, 2012.
3. Wireless Digital Communications - Kamilo Feher - PHI, 2003.
4. Mobile Cellular Communications - W.C.Y. Lee - 2nd Edition, MC Graw Hill, 1995.
4. Wireless Networks - P. Nicopolitidis - Wiley, 2003.
6. Wireless Communications and Networks - William Stallings - 2nd Edition, Prentice Hall of India- 2006.

MODEL QUESTION PAPER – I

Term : V Time : 3Hours

Programme : Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : ELECTIVE THEORY – I Course Code: N1EC404
2. Mobile Communication

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Give examples of wireless communication systems.
2. What is Hand off?
3. Define DVB.
4. Give the services of GSM.
5. What is TETRA?
6. Give the differences between 2.5G and 3G Mobile Communications.
7. Define WAP.
8. What is wireless OS?

PART – B

9. Write short note on Evolution of Mobile Radio Communication.
10. What is meant by Cell Splitting? Explain.
11. Explain Digital Audio broadcasting.
12. Give the frame structure of GSM and explain.
13. Discuss about Forward CDMA channel and reverse CDMA channel.
14. Write about 3G mobile services.
15. Explain tunneling and encapsulation in Mobile IP.
16. Explain Convergence of broadcasting and mobile communication.

[Turn over …..

PART – C

17. (a) Explain in detail Frequency Reuse and Hand off strategies.

(Or)

(b) Discuss about various types of interference in cellular communication.

18. (a) Explain multimedia object transfer protocol with necessary diagrams.

(Or)

(b) Explain in detail DVB.

19. (a) Explain the System Architecture of Global system for Mobile Communication.

(Or)

(b) Explain DECT system architecture with neat diagram.

20. (a) What is GPRS? Explain its system architecture.

(Or)

(b) Explain WAP Protocol architecture.

21. (a) Discuss about Dynamic host configuration protocol in detail.

(Or)

(b) Explain Congestion control methods in detail.

MODEL QUESTION PAPER – II

Term : V Time : 3Hours

Programme : Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : ELECTIVE THEORY – I
2. Mobile Communication Course Code: N1EC404

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. List out the generations of Mobile communication.
2. What is Paging System?
3. Define DVB.
4. Give the features of GSM network.
5. What is UTRAN?
6. What is WAP?
7. Discuss about quality of service in 3G systems.
8. What are the goals of Mobile IP?

PART – B

9. Write short note on Trends in cellular radio and personal Communications.
10. What is meant by sectoring? Explain.
11. Discuss about convergence of broadcasting and mobile communication.
12. Discuss about GSM channel types.
13. What is GPRS and give its features?
14. Explain reverse tunneling in Mobile IP
15. Write about 3G mobile services.
16. Mention the improvements on WCDMA core network.

[Turn over …..

PART – C

17. (a) Write a Detailed notes on any one of wireless Communication systems.

(Or)

(b) Explain Handoff strategies and practical handoff considerations in detail.

18. (a) Explain Digital Audio broadcasting.

(Or)

(b) Explain in detail DVB for high speed Internet access.

19. (a) Explain the Radio Subsystem of GSM.

(Or)

(b) Discuss about Forward CDMA channel and reverse CDMA channel.

20. (a) Explain WAP Protocol architecture in detail.

(Or)

(b) Discuss in detail the 3G CDMA standards in detail.

21. (a) Discuss about Agent discovery protocol in detail.

(Or)

(b) Write about mobile ad-hoc networks.

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(Affiliated to Directorate of Technical Education, Chennai-25)

VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme : Electronics and Communication Engineering
Course code : N1EC405
Term : V
Course Name : ELECTIVE THEORY – I
3. TELEVISION ENGINEERING

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
ELECTIVE THEORY – I 3. TELEVISION ENGINEERING	Hours / Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Hours
I	TV FUNDAMENTALS	16
II	CAMERA AND PICTURE TUBES	15
III	TELEVISION TRANSMITTER	12
IV	TELEVISION RECEIVER	15
V	ADVANCED TELEVISION SYSTEMS	17
	Total	75

Course Outcomes:

On successful completion of the course, the student will be able to:

C405.1	Familiarize the fundamentals of monochrome and color TV.
C405.2	Understand about camera tube & picture tubes and its working.
C405.3	Understand about color TV transmitter.
C405.4	Understand about color TV receiver.
C405.5	Familiarize the LED, LCD displays and fundamentals of CCTV.

Course Outcome linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Teaching Hrs
C405.1	Familiarize the fundamentals of monochrome and color TV.	**R/U/A**	1	16
C405.2	Understand about camera tube & picture tubes and its working.	**R/U/A**	1	15
C405.3	Understand about color TV transmitter.	**R/U/A**	1	12
C405.4	Understand about color TV receiver.	**R/U/A**	1,5	15
C405.5	Familiarize the LED, LCD displays and fundamentals of CCTV.	**R/U/A**	1,2,4,5,7	17
		Total sessions		75

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hour	Max. Marks per Unit	Questions to be set for			Marks weightage (%)
				R	U	A	
I	TV FUNDAMENTALS	16	25	**2**	**18**	**5**	17.86
II	CAMERA AND PICTURE TUBES	15	25	**2**	**18**	**5**	17.86
III	TELEVISION TRANSMITTER	12	25	**2**	**18**	**5**	17.86
IV	TELEVISION RECEIVER	15	25	**2**	**18**	**5**	17.86
V	ADVANCED TELEVISION SYSTEMS	17	25	**2**	**18**	**5**	17.86
I to V*			15	**6**	**9**	**0**	10.70
	Total	75	**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
ELECTIVE THEORY – I 3. TELEVISION ENGINEERING	**3**	**1**	**-**	**1**	**3**	**--**	**1**

Course-PSO Attainment Matrix

Course	Programme Specific Outcomes	
	1	2
ELECTIVE THEORY – I 3. TELEVISION ENGINEERING	**2**	**2**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**TV FUNDAMENTALS:** **MONOCHROME TV:** Basic block diagram of Monochrome TV transmitter and Receiver – Scanning process – horizontal, vertical and sequential scanning – flicker – interlaced scanning (qualitative treatment only) – need for synchronization – blanking pulses – Aspect ratio– Resolution – Types – vertical and horizontal resolution – video bandwidth – composite video signal (CVS)– CVS for one horizontal line – Definitions for Vertical sync pulse, Serrated vertical pulse, Equalizing pulse – Positive & Negative modulation - TV Standards – List of Types of TV standards. **COLOR T.V. FUNDAMENTALS**: Additive mixing of colors – Types – color perception – Chromaticity diagram – Definition for Luminance, Hue, Saturation and Chrominance formation of chrominance signal in PAL system with weighting factors.	**16**
II	**CAMERA AND PICTURE TUBES:** **CAMERA TUBE**: Characteristics – Types of camera tube – working principle of Vidicon and Plumbicon camera tube, CCD camera – Video processing of camera pick up signal – Block diagram and Principle of working of color TV camera tube. **PICTURE TUBE** : Construction and working of Monochrome picture tube – screen phosphor – screen burn – Screen persistence- Aluminized screen – Types of color picture tubes -construction and working principle of Delta gun and Trinitron Color picture tubes – Automatic degaussing	**15**
III	**TELEVISION TRANSMITTER:** Types-Comparision- Principles – Block diagram of Low level IF Modulated TV transmitter – Visual Exciter –Aural Exciter – principle of working of CIN Diplexer – Block diagram of color TV transmitter – color compatibility – PAL color coder –functional blocks and working of each block – Merits and demerits of PAL system.	**12**
IV	**TELEVISION RECEIVER:** Block diagram of Monochrome Receiver – functions of each block – Need for AGC – Advantages of AGC – Video amplifier requirements – High frequency & Low frequency compensation – Block diagram of PAL color Receiver – Need for sync separator – Basic sync separator circuits – Vertical sync separation & Horizontal sync separation – AFC – Need for AFC – Horizontal AFC – Hunting in AFC – Anti Hunt network.	**15**

V	**ADVANCED TELEVISION SYSTEMS:** Block diagram of a digital color TV receiver – Remote control IR transmitter and receiver – Closed Circuit TV system– Applications of CCTV – scrambler – necessity - basic principle- types Descrambler block diagram - Telecine equipment – Digital CCD Telecine system -Introduction to High definition TV (HDTV) and 3DTV. Blue Ray Disc(BD)- The DVD player – Block diagram- Desirable Features & outputs of DVD players-DVD player Models - USB flash drive(pen drive).	**17**

Text Book:

1. Modern Television Practice – Transmission, Reception, Applications R.R.Gulati

   New age international 5th Edition 2015

2. TV and Video Engineeringg. By A.M.Dhake – Second Edition TMH -2003

Reference Book:

1. Monochrome TV Practice, Principles, Technology &servicing by R.R.Gulati-Second Edition- New Age publishers-2004.
2. Monochrome & color TV by R.R.Gulati - New Age publishers -2003.
3. TV &Video Engg. By A.M.Dhake – Second Edition TMH -2003.
4. Color TV, Theory and practice – by S.P.Bali-TMH – 1994.
5. Modern VCD-Video CD Player Introduction, servicing and troubleshooting by Manohar Lotia & Pradeep Nair.

MODEL QUESTION PAPER - I

Term : V Time : 3 Hrs

Programme: Diploma in Electronics and Communication Engineering Max Marks:75

Course : Elective Theory – I Code : N1EC405
3. Television Engineering

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.
(2) Answer division (a) or division (b) of each question in PART – C.
(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. What is scanning?
2. Mention the types of camera tube
3. What is automatic degaussing?
4. What is low level IF modulation?
5. What is the use of visual exciter?
6. What is Anti hunt network?
7. What is HDTV?
8. Give the merits of digital receiver.

PART – B

9. Explain Interlaced scanning.
10. Explain chromaticity diagram.
11. Explain about CCD Camera.
12. Draw the block diagram of PAL colour coder.
13. Explain the principle of working of CIN Diplexer.
14. Draw the block diagram of Monochrome TV receiver.
15. Draw the block diagram of DVD player.
16. Write short notes on blue ray disc

[Turn over …..

PART – C

17. a. Explain a Monochrome TV transmitter with block diagram.

(Or)

b. Explain horizontal and vertical scanning.

18. a. Explain the working of Videocon camera tube with a neat diagram.

(Or)

b. Explain the working of a Delta gun color picture tube.

19. a. Explain working of a PAL color coder with neat diagram.

(Or)

b. With a neat block diagram explain color TV transmitter.

20. a. Draw the block diagram of PAL color TV receiver and explain.

(Or)

b. Explain video amplifier circuit with high frequency and low frequency Compensation.

21. a. Explain the Digital color TV receiver with block diagram.

(Or)

b. Explain the functions of a remote IR transmitter and IR receiver.

MODEL QUESTION PAPER - II

Term : V Time : 3 Hrs

Programme: Diploma in Electronics and Communication Engineering Max Marks: 75

Course : Elective Theory – I Code : N1EC405
3. Television Engineering

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. What is meant by flicker?
2. Mention any two TV standards.
3. Define screen burn.
4. What is the use of CIN diplexer?
5. Define AGC.
6. What is use of tuner section?
7. What is HDTV?
8. What is 3DTV?

PART – B

9. Explain Composite video signal.
10. Explain Positive & Negative modulation.
11. What is mean by Aluminized screen?
12. Draw the block diagram of color TV Camera Tube.
13. Explain Aural Exciter.
14. Explain the Need for sync separator.
15. Draw the block diagram of Digital CCD telecine system.
16. Explain the Applications of CCTV.

[Turn over …..

PART – C

17. a) Explain a Monochrome TV receiver with block diagram.

(Or)

b) Explain Sequential and vertical scanning.

18. a) Explain the working of Plumbicon camera tube with a neat diagram.

(Or)

b) Explain the working of a Trinitron Color picture tubes.

19. a) Explain the Block diagram of Low level IF Modulated TV transmitter.

(Or)

b) Explain the Merits and demerits of PAL system.

20. a) Draw and explain the Block diagram of Monochrome Receiver .

(Or)

b) Explain video amplifier circuit with high frequency and low frequency Compensation.

21. a) Draw and explain closed circuit TV system.

(Or)

b) Explain the functions of a remote IR transmitter and IR receiver.

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VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme : Diploma in Electronics and communication Engineering

Course code : N1EC311

Term : V

Course Name : ADVANCED COMMUNICATION SYSTEMS PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
Advanced Communication Systems Practical	Hours / Week	Hours / Term	Marks			Duration
	4	60	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C311.1	Analyze digital modulation techniques and Sampling, Multiplexing
C311.2	Demonstrate OFC characteristics & applications.
C311.3	Analyze the Encoding and Decoding techniques
C311.4	Install and test Transmitting and receiving systems.

Course Outcome linkage to Cognitive Level:

On successful completion of the course, the students will be able to attain following Course Outcomes

Course Outcome		Experiment linked	CL	Linked PO	Teaching Hrs
C311.1	Analyze digital modulation techniques and Sampling, Multiplexing	1,2,3,4,6	U,A	1,2	18
C311.2	Demonstrate OFC characteristics & applications.	10,11,12,14,15	U,A	1,2,4	20
C311.3	Analyze the Encoding and Decoding techniques	7,13	U,A	1,2,4	8
C311.4	Install and test Transmitting and receiving systems.	5,9,16	U,A	1,4	14
			Total sessions		**60**

Legends: R = Remember U= Understand; A= Application and above levels (Bloom's revised taxonomy)

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
ADVANCED COMMUNICATION SYSTEMS PRACTICAL	**3**	**3**	**-**	**3**	**--**	**--**	**--**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

LIST OF EXERCISES

1.Construct analog signal sampling and reconstruction circuit to prove sampling theorem.

2.Trace the output waveform of a ASK modulation and demodulation circuit.

3.Trace the output waveform of a FSK modulation and demodulation circuit.

4.Trace the output waveform of a PSK modulation and demodulation circuit.

5. Simulate the ASK Modulation and demodulation using the simulation tool like PSPICE/ multisim/orcad/tina

6.Simulate the FSK Modulation and demodulation using the simulation tool like PSPICE/ multisim/orcad/tina

7.Simulate the PSK Modulation and demodulation using the simulation tool like PSPICE/ multisim/orcad/tina

8.Determine the output waveforms of TDM and de-multiplexing circuit.

9.Trace the output waveform of PCM signal.

10. Set up fiber optic communication interface to COM port of a computer and test its performance.

11. Set up and test a fiber optic analog link

12. Set up and test a fiber optic digital link.

13. Measure the bending loss and propagation loss in fiber optics.

14. Test the performance of Manchester encoder and decoder.

15. Measure the Numerical aperture of optical fiber.

16. Install & test a DTH system.

17. Splicing the Optical Fibers. **(Not for examination)**

LIST OF EQUIPMENTS

HARDWARE REQUIRMENT:

Sl. No.	Name of the Equipments	Range	Required Nos.
1.	Regulated power supply	0-30V	5
2.	Dual trace CRO	-	2
3.	Signal Generator	1MHz	1
4.	Fiber optics kit	-	2
5.	PCM trainer KIT	-	1
6.	ASK modulation &demodulation kit	-	1
7.	PSK modulation &demodulation kit	-	1
8.	FSK modulation &demodulation kit	-	1
9.	TDM kit	-	1
10.	Analog signal sampling and reconstruction kit	-	1
11.	DTH kit and parabolic antenna	-	1
12.	Desktop/laptop computers	-	2

SIMULATION SOFTWARE REQUIREMENT:

1. MULTISIM.

Detailed Allocation of Marks for External Assessment

Scheme of valuation in TEE		
1.	Circuit Diagram	20
2.	Connection	25
3.	Execution& Handling of Equipment	15
4.	Result/Output	10
5.	Viva-voce	05
	Total	**75**

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VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC312

Term : V

Course Name : MICROCONTROLLER PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
MICRO CONTROLLER PRACTICAL	Hours / Week	Hours / Term	Marks			Duration
	4	60	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C 312.1	Develop programming of 8051 Micro controller based on its architecture and instruction set.
C 312.2	Design and implement peripheral devices interfacing with 8051 MC.
C 312.3	Design Serial Communication & Real Time applications.
C 312.4	Develop installation of Android OS.

Course Outcome linkage to Cognitive Level:

On successful completion of the course, the students will be able to attain following Course Outcomes

Course Outcome		Experiment linked	CL	Linked PO	Teaching Hrs
C312.1	Develop programming of 8051 Micro controller based on its architecture and instruction set	Part- A 1,2,3,4,5,6,	R,U	1, 2, 4	24
C312.2	Design and implement peripheral devices interfacing with 8051 MC.	Part – B 1,2,3,4,5,6	U,A	1, 2, 3	29
C312.3	Design Serial Communication & Real Time applications.	Part-A, Part- B 7,7	U,A	1, 2, 3	4
C312.4	Develop Installation of Android OS.	Part – C 1	R,U	1	3
			Total sessions		**60**

Legends: R = Remember U= Understand; A= Application and above levels (Bloom's revised taxonomy)

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
MICRO CONTROLLER PRACTICAL	**3**	**3**	**2**	**2**	**-**	**-**	**-**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

LIST OF EXERCISES

The programs may be executed by using 8051 kit / Keil IDE simulator tool.

Part - A

1. Write an Assembly Language Program for Multiplication and Division of two numbers and execute.

2. Write an Assembly Language Program for Multi-byte Addition and execute.

3. Write an Assembly Language Program to find the Largest / Smallest number.

4. Write an Assembly Language Program for arranging the given data in Ascending / Descending order and execute.

5. Write an Assembly Language Program for ASCII to Binary and execute.

6. Write an Assembly Language Program for Odd / Even Parity bit generation and execute.

7. Write an Assembly Language Program for using timer / Counter and execute.

Part - B

INTERFACING WITH APPLICATION BOARDS

1. Write an Assembly Language / C Program for interfacing Digital I/O board and test it.

2. Write an Assembly Language / C Program for interfacing seven segment LED display and test it.

3. Write an Assembly Language / C Program for interfacing 8 bit ADC and test it.

4. Write an Assembly Language / C Program for interfacing 8 bit DAC and test it.

5. Write an Assembly Language / C Program for interfacing STEPPER MOTOR and test it.

6. Write an Assembly Language / C Program for interfacing DC motor and test it.

7. Write an Assembly Language / C Program for sending data through serial port between controller kits and test it.

8. Write an Assembly Language / C Program for Keyboard interface.

Part - C

1. Study of Android operating system installation. **(Not for Examination)**

LIST OF EQUIPMENTS REQUIRED

Sl. No.	Name of the Equipments	Required Nos.
1.	8051 Microcontroller Kit	10
2.	Digital I/O Interface Board	2
3.	Keyboard Interface Board	2
4.	Seven segment LED display Interface Board	2
5.	8 bit ADC Interface Board	2
6.	8 bit DAC Interface Board	2
7.	Stepper motor Interface Board	2
8.	DC motor control Interface Board	2
9.	8051 Development Board with connector	5
10.	Android SDK Tool kit	1

Detailed Allocation of Marks for External Assessment

SL.No.	DESCRIPTION	MAX. MARK
1.	Program	30
2.	Debugging and execution	30
3.	Result	10
4.	Viva-voce	05
TOTAL		**75**

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VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC313

Term : V

Course Name : Very Large Scale Integration Practical

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
Very Large Scale Integration Practical	Hours / Week	Hours / Term	Marks			Duration
	4	60	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

Code	**Course Outcomes**
C313.1	Write VHDL Program(codes) for Combinational & Arithmetic Circuits.
C313.2	Write VHDL Program(codes) for Sequential Circuits.
C313.3	Write VHDL Program(codes) for 7 Segment LEDs& Logic Gates.
C313.4	Design a Schematic entry Diagram using VHDL code.

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		Experiment linked	CL	Linked PO	Linked PSO	Teaching Hrs
C313.1	Write VHDL Program(codes) for Combinational & Arithmetic Circuits.	**1,2**	**U,A**	2,3,4,5	1,2	**08**
C313.2	Write VHDL Program(codes) for Sequential Circuits.	**3,4,5,6,9**	**U,A**	2,3,4,5	2	**20**
C313.3	Write VHDL Program(codes) for 7 Segment LEDs & Logic Gates.	**7,8,10,11,12**	**U,A**	2,3,4,5	2	**20**
C313.4	Design a Schematic entry Diagram using VHDL code.	**13,14,15**	**A**	2,3,4	2	**12**
			Total sessions			**60**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
VERY LARGE SCALE INTEGRATION PRACTICAL	**-**	**3**	**3**	**3**	**2**	**-**	**-**

Course-PSO Attainment Matrix:

Course	Programme Specific Outcomes	
	1	2
Very Large Scale Integration Practical	**-**	**3**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

LIST OF EXERCISES

1. SIMULATION OF VHDL CODE FOR COMBINATIONAL CIRCUIT

Optimize a 4 variable combinational function (SOP or POS), describe it in VHDL code and simulate it.

Example: F= (0,5,8,9,12) in sop or pos

2. SIMULATION OF VHDL CODE FOR ARITHMETIC CIRCUITS

Design and Develop the circuit for the following arithmetic function in VHDL Codes and Simulate it. Addition, Subtraction, Multiplication (4 x 4 bits)

3. SIMULATION OF VHDL CODE FOR MULTIPLEXER

Design and develop a 2 bit multiplexer and portmap the same for developing upto 8 bit multiplexer.

4. SIMULATION OF VHDL CODE FOR DEMULTIPLEXER

Design and develop an 8 output demultiplexer. Simulate the same code in the software

5. VHDL IMPLEMENTATION OF MULTIPLEXER

Describe the code for a multiplexer and implement it in FPGA kit in which switches are connected for select input and for data inputs. A LED is connected to the output.

6. VHDL IMPLEMENTATION OF DEMULTIPLEXER

Switches are connected for select inputs and a data input, Eight LEDs are connected to the output of the circuit.

7. VHDL IMPLEMENTATION OF 7 SEGMENT DECODER

Develop Boolean expression for 4 input variables and 7 output variables.

Design and develop a seven segment decoder in VHDL for 7 equations. A seven segment display is connected to the output of the circuit. Four switches are connected to the input. The 4 bit input is decoded to 7 segment equivalent.

8. VHDL IMPLEMENTATION OF 7 SEGMENT DECODER BY LUT

Develop a 7 segment decoder using Look up table. Describe the seven segment decoder in VHDL using developed Look up table. A seven segment display is connected to the output of the circuit. Four switches are connected to the input. The 4 bit input is decoded into 7 segment equivalent.

9. VHDL IMPLEMENTATION OF ENCODER

Design and develop HDL code for decimal (Octal) to BCD encoder. There will be10 input switches (or 8 switches) and 4 LEDs in the FPGA kit. The input given from switches and it is noted that any one of the switch is active. The binary equivalent for the corresponding input switch will be glowing in the LED as output.

10. SIMULATION OF VHDL CODE FOR DELAY

Develop a VHDL code for making a delayed output for 1second or 2 seconds by assuming clock frequency provided in the FPGA Kit.

11. VHDL IMPLEMENTATION FOR BLINKING A LED

Develop a VHDL Code for delay and verify by simulating it. This delay output is connected to LED. Delay is adjusted such away LED blinks for every 1 or 2 seconds.

12. SIMULATE A VHDL TEST BENCH CODE FOR TESTING A GATE, COUNTER

Develop a VHDL test bench code for testing any one of the simple gate and counter. Simulate the test bench code in the HDL software.

13. VHDL IMPLEMENTATION FOR BLINKING A ARRAY OF LEDS

Design and develop a VHDL Code for 4 bit binary up counter. Four LEDs are connected at the output of the counter. The counter should up for every one second.

14. VHDL IMPLEMENTATION OF A SPELLER WITH 7 SEGMENT DISPLAY

Design and develop VHDL Code for a 4 Letter Word (Seven segment display) The LEDs are connected at the output of the counter. The speller should work for every one seconds.

15. VHDL IMPLEMENTATION OF 7 SEGMENT DISPLAY

Design and develop a seven segment decoder in VHDL. Design and develop a 4 bit BCD counter, the output of the counter is given to seven segment decoder. A seven segment display is connected to the output of the decoder. The display shows 0,1, 2.. 9 for every one second.

Content Beyond Syllabus :

- Construct a Test Bench for 3 bit Ripple counter using VHDL code and simulate .

LIST OF EQUIPMENTS:

1. FPGA KIT with atleast 10 switches for input, 8 LEDs for output, a 7 segment display, debounced push switch (2 Nos) for manual clock input and external clock source – 10Nos.
2. Desktop Computers -.10 Nos.

Manual for the FPGA Kit and interface kit can be given to students for the final exam.

END EXAMINATION :

Note : In the End Examination, all the experiments have to be given and the students have to select one experiment based on the lot.

ALLOCATION OF MARKS:

SL.NO.	ALLOCATION	MARKS
1.	Program Writing	35
2.	Debugging & Execution	30
3.	Result	05
4.	Viva-voce	05
	Total	**75**

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(Affiliated to Directorate of Technical Education, Chennai-25)

VIRUDHUNAGAR – 626 001

N1 - SCHEME

Programme : Diploma in Electronics and communication Engineering

Course code : N1EC307

Term : VI

Course Name : Computer Hardware Servicing and Networking

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
Computer Hardware Servicing and Networking	Hours / Week	Hours / Term	Marks			Duration
	6	90	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Hours
1.	MOTHERBOARD COMPONENTS AND MEMORY STORAGE DEVICES	18
2.	I/O DEVICES AND INTERFACE	18
3.	MAINTENANCE AND TROUBLE SHOOTING OF DESKTOP AND LAPTOPS	18
4.	COMPUTER NETWORK DEVICES AND OSI LAYERS	18
5.	802.X AND TCP/IP PROTOCOLS	18
	Total	90

Course Outcomes:

On successful completion of the course, the student will be able to:

C307.1	Describe the various mother board components and memory storage devices.
C307.2	Understand the interfacing of I/O devices with computer
C307.3	Demonstrate the maintenance and trouble shooting of desktop and laptop
C307.4	Explain the different types of networks and OSI model
C307.5	Describe the 802.X and TCP/IP Protocols

Course Outcome linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		**CL**	**Linked PO**	**Teaching Hrs.**
C307.1	Describe the various mother board components and memory storage devices.	***R/U/A***	1	18
C307.2	Understand the interfacing of I/O devices with computer.	***R/U/A***	2,3	18
C307.3	Demonstrate the maintenance and trouble shooting of desktop and laptop.	***R/U/A***	2,3,5	18
C307.4	Explain the different types of networks and OSI model.	***R/U/A***	1,5	18
C307.5	Describe the 802.X and TCP/IP Protocols	***R/U/A***	2,3	18
		Total sessions		90

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	MOTHERBOARD COMPONENTS AND MEMORY STORAGE DEVICES	18	25	**2**	**18**	**5**	17.86
II	I/O DEVICES AND INTERFACE	18	25	**2**	**18**	**5**	17.86
III	MAINTENANCE AND TROUBLE SHOOTING OF DESKTOP AND LAPTOPS	18	25	**2**	**18**	**5**	17.86
IV	COMPUTER NETWORK DEVICES AND OSI LAYERS	18	25	**2**	**18**	**5**	17.86
V	802.X AND TCP/IP PROTOCOLS	18	25	**2**	**18**	**5**	17.86
I to V *			**15**	**6**	**9**	**0**	**10.70**
	Total	**90**	**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
Computer Hardware Servicing and Networking	**1**	**3**	**3**	**-**	**3**	**--**	**--**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

UNIT	NAME OF THE TOPIC	HOURS
I	**MOTHERBOARD COMPONENTS AND MEMORY STORAGE DEVICES** **Introduction:** Hardware, Software and Firmware. Mother board, IO and memory expansion slots, SMPS, Drives, front panel and rear panel connectors. **Processors:** Architecture and block diagram of multi core Processor, Features of new processor(Definition only)-chipsets (Concepts only) **Bus Standards:** Overview and features of PCI, AGP, PCMCIA **Primary Memory**: Introduction-Main Memory, Cache memory – DDR2, DDR3 and Direct RDRAM. **Secondary Storage:** Hard Disk – Construction – Working Principle Specification of IDE, Ultra ATA, Serial ATA; HDD Partition - Formatting. **Removable Storage:** Solid State Memory Devices (SSD), CD-R, CD-RW, DVD –ROM and DVD –RW**:** construction and reading& writing operations; Blue-ray – Introduction –Disc Parameters.	18
II	**I/O DEVICES AND INTERFACE** **Keyboard:** Signals – operation of membrane and mechanical keyboards–troubleshooting; wireless Keyboard. **Mouse:** types, connectors, operation of Optical mouse and Troubleshooting. **Printers**: Introduction – Types of printers- Dot Matrix, Inkjet, Laser, MFP (Multi Function Printer) and Thermal printer – Operation, Construction and Features-Troubleshooting **Scanner:** Types-Operation-Scan resolution-Scan modes. **I/O Ports:** Serial, Parallel, USB, Game Port and HDMI. **Displays:** Principles of LED, LCD and TFT Displays. **Graphic Cards:** VGA and SVGA card. **Modem:** Working principle. **Power Supply:** Servo Stabilizers, online and offline UPS – working Principles; SMPS: Principles of Operation and block diagram of ATX Power supply, Connector Specifications.	18
III	**MAINTENANCE AND TROUBLE SHOOTING OF DESKTOP AND LAPTOPS** **Bios-setup:** Standard CMOS setup, Advanced BIOS setup, Power management, advanced chipset features, PC Bios communication – upgrading BIOS, Flash BIOS -setup. **POST:** Definition – IPL hardware – POST Test sequence – beep codes **Diagnostic Software and Viruses:** Computer Viruses – Precautions – Anti-virus Software – identifying the signature of viruses – Firewalls and latest diagnostic softwares. **Laptop:** Types of laptop –block diagram – working principles– configuring laptops and power settings -SMD components, ESD and precautions. **Laptop components:** Adapter – types, Battery – types, Laptop Mother Board - block diagram,Laptop Keyboard and Touchpad .	18

	Installation and Troubleshooting: Formatting, Partitioning and Installation of OS – Trouble Shooting Laptop Hardware problems - **Preventive maintenance techniques for laptops.**	
IV	**COMPUTER NETWORK DEVICES AND OSI LAYERS** **Data Communication:** Components of a data communication. **Data flow:** simplex – half duplex – full duplex **Topologies:** Star,Bus, Ring, Mesh, Hybrid – Advantages and Disadvantages of each topology. **Networks: Definition** -Types of Networks: LAN – MAN – WAN – CAN – HAN – Internet –Intranet –Extranet, Client-Server, Peer To Peer Networks. **Network devices:** Features and concepts of Switches – Routers(Wired and Wireless) – Gateways. **Network Models:** Protocol definition - standards - OSI Model – layered architecture – functions of all layers.	18
V	**802.X AND TCP/IP PROTOCOLS** **Overview of TCP / IP**: TCP/IP – Transport Layers Protocol – connection oriented and connectionless Services – Sockets - TCP & UDP. **802.X Protocols :** Concepts and PDU format of CSMA/CD (802.3) – Token bus (802.4) – Token ring (802.5) – Ethernet – type of Ethernet (Fast Ethernet, gigabit Ethernet) – Comparison between 802.3, 802.4 and 802.5 **Network Layers Protocol:** IP –Interior Gateway Protocols (IGMP, ICMP, ARP, RARP Concept only). **IPv4 Addressing :** Dotted Decimal Notation –Subnetting & Supernetting. **Application Layer Protocols:** FTP– Telnet – SMTP– HTTP – DNS - POP	18

Text Book:

1. IBM PC and CLONES, B.Govindrajalu, Tata McGrawhill Publishers.
2. Computer Installation and Servicing, D.Balasubramanian, Tata McGraw Hill
3. The complete PC upgrade and Maintenance, Mark Minasi, BPB Publication.
4. Troubleshooting, Maintaining and Repairing PCs, Stephen J Bigelow ,Tata McGraw Hill Publication.
5. Upgrading and repairing laptops, Scott Mueller, QUE Publication.
6. Data Communication and networking, Behrouz A.Forouzan, Tata Mc-Graw Hill, New Delhi,
7. Data and Computer Communications, William Stallings, Prentice-Hall of India, Eighth Edition
8. Computer Networks, Andrew S.Tanenbaum, Prentice-Hall of India, New Delhi,

Reference Book:

1.Computer Networks,Achyut Godbole,Tata Mc-Graw Hill -New Delhi.

2. Principles of Wireless Networks– A unified Approach, Kaveh Pahlavan and Prashant Krishnamurty, Pearson Education, 2002.

MODEL QUESTION PAPER – I

Term : VI Time : 3 Hrs

Programme : Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : Computer Hardware Servicing and Networking Course Code : N1EC307

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. What is chipset?
2. Define Direct RDRAM.
3. What are membrane and mechanical keyboards?
4. List out the types of printers.
5. Define BIOS.
6. Give the types of RAM.
7. Define LAN and MAN.
8. Define Networks.

PART – B

9. What is the difference between Hardware, Software and Firmware?
10. Draw the PCI block diagram.
11. Explain in detail about SVGA.
12. Explain Power Management.
13. Write down the steps involved in OS installation.
14. What is dotted decimal notation? Give example.
15. Explain about SMTP.
16. What is client server network?

[Turn over …..

PART – C

17. (a) Explain in detail about the architecture of Multi Core Processor with neat diagram.

(Or)

(b) Give detailed notes on Primary Memory.

18. (a) Explain the working principle of MODEM.

(Or)

(b) Explain the construction and operation of laser printer.

19. (a) What are the signatures of Viruses? How can we protect the system by Firewall and latest diagnostic softwares?

(Or)

(b) What is POST? List out the tests performed by POST.

20. (a) Explain in detail about OSI model with neat diagram.

(Or)

(b) Explain in detail about Network Devices.

21. (a) Explain in detail about TCP and UDP.

(Or)

(b) Explain about Telnet and FTP.

MODEL QUESTION PAPER - II

Term : VI — Time : 3 Hrs

Programme : Diploma in Electronics and Communication Engineering — Max. Marks : 75

Course : Computer Hardware Servicing and Networking — Course Code : N1EC307

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. What is acronym of SMPS?
2. What is PCI?
3. What is acronym USB?
4. What are TFT displays?
5. What is POST?
6. What is acronym of SMD?
7. What is Peer to Peer network?
8. What is Telnet?

PART – B

9. What is AGP?
10. What is Cache Memory?
11. What are the different types of Graphics cards?
12. What is the use of Touch Pad?
13. What is Star Topology?
14. What is CAN?
15. What is ICMP protocol?
16. What is Gigabit Ethernet?

[Turn over …..

PART – C

17. (a) Explain the working principles of Solid State Memory Devices.

(Or)

(b) Explain the working principles of Blue-ray disk.

18. (a) Explain the operation of Dot matrix printer with diagram.

(Or)

(b) Explain the working principle of MODEM

19. (a) Explain the significance of advanced BIOS setup.

(Or)

(b) Draw and explain layout of laptop motherboard.

20. (a) Discuss about the components of Data Communication.

(Or)

(b) Discuss about Half duplex and Full duplex communication.

21. (a) Discuss about Connection oriented and connectionless protocol services.

(Or)

(b) Discuss about the significance of HTTP.

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VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC308

Term : VI

Course Name : BIOMEDICAL INSTRUMENTATION

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
BIOMEDICAL INSTRUMENTATION	Hours / Week	Hours / Term	Marks			Duration
	6	90	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Time in Hrs
1	Bio-Electric Signals and Electrodes and Clinical	18
2	Bio-Medical Recorders	18
3	Therapeutic Instruments	18
4	Biotelemetry and Patient Safety	18
5	Modern Imaging Technique	18
	Total	90

Course Outcomes:

On successful completion of the course, the student will be able to:

C308.1	Gain knowledge of different types of measurements in medical field.
C308.2	Familiarize the recorders in medical field.
C308.3	Understand the use of therapeutic instruments.
C308.4	know about the biotelemetry and patient safety.
C308.5	know about the modern imaging techniques.

Course Outcome linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Teaching Hrs.
C308.1	Gain knowledge of different types of measurements in medical field.	**R/U/A**	1,2,5	18
C308.2	Familiarize the recorders in medical field.	**R/U/A**	1,2,5,7	18
C308.3	Understand the use of therapeutic instruments.	**R/U/A**	1,2,5	18
C308.4	know about the biotelemetry and patient safety.	**R/U/A**	1,2,5	18
C308.5	know about the modern imaging techniques.	**R/U/A**	1,2,5	18
		Total sessions		90

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	Bio-Electric Signals and Electrodes and Clinical Measurement	**18**	25	**2**	**18**	**5**	17.86
II	Bio-Medical Recorders	**18**	25	**2**	**18**	**5**	17.86
III	Therapeutic Instruments	**18**	25	**2**	**18**	**5**	17.86
IV	Biotelemetry and Patient Safety	**18**	25	**2**	**18**	**5**	17.86
V	Modern Imaging Technique	**18**	25	**2**	**18**	**5**	17.86
I to V *****			15	**6**	**9**	**0**	10.70
	Total	**90**	**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
BIOMEDICAL INSTRUMENTATION	**3**	**3**	**-**	**-**	**3**	**-**	**1**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**BIO-ELECTRIC SIGNALS AND ELECTRODES AND CLINICAL MEASUREMENT** **BIO-ELECTRIC SIGNALS AND ELECTRODES** Elementary ideas of cell structure, Bio – potential and their generation – resting and action potential – propagation of action potential. Electrodes – Micro – Skin surface – needle electrodes. **CLINICAL MEASUREMENT** Measurement of Blood pressure (direct, indirect) – blood flow meter (Electromagnetic & ultrasonic blood flow meter) – blood pH measurement - Measurement of Respiration rate – measurement of lung volume – heart rate measurement – Measurement of body and skin temperature - Chromatography, Photometry, Flurometry.	18
II	**BIO - MEDICAL RECORDERS** Electro cardiograph (ECG) – Lead system – ECG electrodes – ECG amplifiers – ECG recording units – analysis of ECG curves. Nervous system – EEG recorder – 10-20 lead system – recording techniques – EEG wave types – Clinical use of EEG – brain tumor – Electro – myograph (EMG) – EMG waves – measurement of conduction velocity – EMG recording techniques – Electro – retinograph (ERG) Audiometer – principle – types – Basics audiometer working.	18
III	**THERAPEUTIC INSTRUMENTS** Cardiac pacemaker – classification – External pacemakers – implantable pacemaker – pacing techniques – programmable pacemaker – Cardiac defibrillators – types – AC and DC defibrillators Heart lung machine with Block diagram. Dialysis – Hemodialysis – peritoneal dialysis. Endoscopes Endoscopic laser coagulator and applications – physiotherapy equipment – short wave diathermy – microwave diathermy – ultrasonic therapy unit (block / circuit) – Ventilators – types – modern ventilator block diagram.	18
IV	**BIOTELEMETRY AND PATIENT SAFETY** Introduction to biotelemetry – physiological – adaptable to biotelemetry – components of a biotelemetry system – application of telemetry – elements of biotelemetry; AM, FM transmitter and receiver – requirements for biotelemetry system – radio telemetry with sub carrier – single channel and multi channel telemetry – Telemedicine; introduction, working, applications. **Patient safety:** Physiological effects of electric current – Micro and macro shock – leakage current – shock hazards from electrical equipment. Methods of Accident Prevention – Grounding – Double Insulation – Protection by low voltage – Ground fault circuit interrupter – Isolation of patient connected parts – Isolated power distribution system. Safety aspects in electro surgical units – burns, high frequency current hazards, Explosion hazards.	18

V	**MODERN IMAGING TECHNIQUES** LASER beam properties – block diagram – operation of CO_2 and NDYag LASER – applications of LASER in medicine. X-ray apparatus – block diagram – operation – special techniques in X-ray imaging – Tomogram – computerized Axial tomography – Ultrasonic imaging techniques – Echo cardiography – Angiography – CT scanner- Magnetic Resonance Imaging techniques.	18

Text Book:

1. Dr. M. Arumugam – Biomedical Instrumentation, Anuradha Publications, Chennai

Reference Books.

1. Leslie Cromwell –Fred J. Wibell, Erich A.Pfeiffer – Biomedical Instrumentation and measurements, II Edition.
2. Jacobson and Webstar – Medicine and clinical Engineering.
3. R.S. Khandpur – Hand book of Bio –Medical Instrumentation.
4. Medical Electronics - Kumara Doss
5. Introduction to Medical Electronics. B.R. Klin
6. Introduction to Biomedical Instrumentation, Mandeep Singh, Printice Hall ndia 2010.

MODEL QUESTION PAPER – I

Term	: VI	Time	: 3 Hrs
Programme	: Diploma in Electronics and Communication Engineering	Max Marks	: 75
Course	: Biomedical Instrumentation	Code	: N1EC308

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q. No. 8 in PART – A and Q. No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define action potential.
2. What is meant by respiration rate?
3. What is an audiometer?
4. Expand EMG, ERG, EEG.
5. What is fibrillation?
6. What is micro shock?
7. What is angiography
8. State the applications of CT scan.

PART – B

9. Explain the cell structure with diagram.
10. Explain about ECG amplifier.
11. Draw the EEG waveforms.
12. Explain about DC defibrillator.
13. Explain the need for pacemaker.
14. Write the methods of accident prevention.
15. Define biotelemetry.
16. Write any two laser properties.

[Turn over …..

PART – C

17. a) Explain different types of electrode with diagram.

(Or)

b) Explain any one blood flow meter with diagram.

18. a) Explain 10-20 lead system with diagram.

(Or)

b) Explain ECG recording technique with diagram.

19. a) Explain programmable pacemaker with diagram.

(Or)

b) Explain endoscopic laser coagulator with diagram.

20. a) Explain telemedicine with diagram.

(Or)

b) Explain methods of accident prevention with diagram.

21. a) Explain operation of CO_2 and NDYag laser with diagram.

(Or)

b) Explain MRI scan with diagram.

MODEL QUESTION PAPER – II

Term	: VI	Time	: 3 Hrs
Programme	: Diploma in Electronics and Communication Engineering	Max Marks	: 75
Course	: Biomedical Instrumentation	Code	: N1EC308

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q. No. 8 in PART – A and Q. No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. Define resting potential.
2. Define blood pH.
3. What is ECG?
4. What do you mean by dialysis?
5. List the different methods of telemedicine
6. State the different types of leakage current
7. What are the applications of LASER in medical field?
8. How MRI scan is superior than other scan?

PART – B

9. Write short notes on needle electrodes.
10. Explain about ECG amplifier.
11. Draw the block diagram of EEG recording unit.
12. Explain about AC defibrillator.
13. Write short notes on Hemo dialysis.
14. What are the different causes for shock hazard?
15. Define biotelemetry.
16. Write short notes on angiography.

[Turn over …..

PART – C

17. a) Explain Ultrasonic blood flow meter with neat diagram.

(Or)

b) Explain the measurement of heart rate with neat diagram.

18. a) Explain ERG recording technique with diagram.

(Or)

b) Explain EMG recording technique with diagram.

19. a) What is pacing and discuss in detail about different pacing techniques.

(Or)

b) Explain the working of Heart lung machine with neat diagram.

20. a) Explain the biotelemetry system with its block diagram.

(Or)

b) Describe in detail about shock hazards from electrical equipments.

21. a) Explain operation of CT scanner with neat diagram.

(Or)

b) Explain the working of echocardiography with diagram.

VIRUDHUNAGAR S.VELLAICHAMY NADAR POLYTECHNIC COLLEGE (AUTONOMOUS)

(Affiliated to Directorate of Technical Education, Chennai-25)

VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC407

Term : VI

Course Name : ELECTIVE THEORY – II

1. EMBEDDED SYSTEMS

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
	Hours / Week	Hours / Term	Marks			Duration
ELECTIVE THEORY – II 1. EMBEDDED SYSTEMS	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Time in Hrs
1.	ARM Embedded System	15
2.	ARM Processor Fundamentals	15
3.	LPC2148 Architecture –I	15
4.	LPC2148 Architecture –II	15
5.	Real Time Operating System	15
	Total	**75**

Course Outcomes:

On successful completion of the course, the student will be able to:

C407.1	Understand the ARM Processor Fundamentals.
C407.2	Understand the ARM Processor Instruction set.
C407.3	Understand the ARM based Embedded Microcontroller. (LPC2148 Features, GPIO,VPB,VIC)
C407.4	Understand the LPC2148 Features like UART, I^2C, PWM.
C407.5	Understand Real Time Operating System.

Course Outcome linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Linked PSO	Teaching Hrs.
C407.1	Understand the ARM Processor Fundamentals.	***R/U/A***	1	2	15
C407.2	Understand the ARM Processor Instruction set.	***R/U/A***	1,2	2	15
C407.3	Understand the ARM based Embedded Microcontroller. (LPC2148 Features, GPIO,VPB,VIC)	***R/U/A***	1,2,3	2	15
C407.4	Understand the LPC2148 Features like UART, I^2C, PWM.	***R/U/A***	1,2,3	1,2	15
C407.5	Understand Real Time Operating System.	***R/U/A***	1,7	2	15
		Total sessions			75

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	ARM Embedded System	15	25	**2**	**18**	**5**	17.86
II	ARM Processor Fundamentals	15	25	**2**	**18**	**5**	17.86
III	LPC2148 Architecture –I	15	25	**2**	**18**	**5**	17.86
IV	LPC2148 Architecture –II	15	25	**2**	**18**	**5**	17.86
V	Real Time Operating System	15	25	**2**	**18**	**5**	17.86
I to V *			15	**6**	**9**	**0**	10.70
	Total	75	**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
ELECTIVE THEORY – II 1. EMBEDDED SYSTEMS	**3**	**2**	**2**	**1**	**-**	**-**	**1**

Course-PSO Attainment Matrix:

Course Name	Programme Specific Outcomes	
	1	2
ELECTIVE THEORY – II 1. EMBEDDED SYSTEMS	**1**	**3**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**ARM EMBEDDED SYSTEM** Introduction to ARM – Features of ARM which makes ARM suitable for Embedded systems- Structure of a typical embedded device based on ARM Processor core - Comparison of various ARM Families- AMBA bus- Memory model: VonNeumann and Harvard- ARM core Dataflow model- ARM 7 TDMI features- ARM7 functional block diagram- ARM7 internal structure- ARM7 operating states- Applications of ARM processor- Programming software tools -Code development flowchart- Assembler, Compiler, Simulator, Emulator, Loader, Linker, Debugger.	15
II	**ARM PROCESSOR FUNDAMENTALS** ARM Registers: GPR, PC, CPSR,SPSR ,LR registers- Structure of CPSR- Banked registers - ARM processor Operating modes- 3-stage pipelining of ARM7-Memory and Memory Interface-Exceptions- Action on entering and leaving an exception- Exception priority-ARM instruction set- Data processing instructions- MOV & MVN instructions- Barrel shifter- Arithmetic instructions like ADD, ADC, RSB, SUB, SBC and RSC- Logical instructions like AND,ORR,EOR,BIC- Comparison instructions like CMP, TEQ, TST, CMN- Multiply instructions like MLA, MUL, UMULL, UMLAL, SMULL, SMLAL - Load and Store instructions like LDR, LDRB, LDRH, LDRSB, LDRSH, STR, STRB, STRH, LDM and STM- Pre and Post indexed with / without write back-addressing modes for multiple data transfer-Stack operations using STM &LDM instructions- Branch instructions like B,BL,BX and BLX-SWAP, Software interrupt and PSR instructions - THUMB state - change from ARM state to THUMB state using BX and BLX instruction.	15
III	**LPC2148 ARCHITECTURE – I** ARM based Embedded Microcontroller – LPC 2148 Block Diagram and features – On chip program memory - On chip static RAM-Memory mapping-Pin Connect Block – General Purpose Input Output (GPIO) - Features, Application, Registers (IODIR,IOSET,IOCLR,IOPIN) - PLL- Introduction, Registers, PLL frequency calculation - VPB Divider - Brownout detector - Reset and Wakeup Timer - Description of Vectored Interrupt Controller (VIC).	15

IV	**LPC2148 ARCHITECTURE–II** LPC 2148 Timer : Features, Registers (TCR,CTCR,TC,PR,PC), UART: Features, Registers (UTHR,URBR, UDLL and UDLM,ULCR,ULSR), Analog Interfacing: ADC- Features, ADC Registers (ADCR,ADGDR,ADSTAT,ADGSR,ADINTEN,ADDR), DAC – Features, DAC register, I^2C Features and Operating Modes, Registers (I2CONSET, I2CONCLR, I2STAT, I2DAT, I2ADR, I2SCLL, I2SCLH) -SPI (Features only), SSP (Features only), USB (Features only) – PWM Features- Description - Single edge and Double edge PWM- RTC (Features only).	15
V	**REAL TIME OPERATING SYSTEM** Definition of RTOS – Comparison with general OS – Soft and Hard RTOS – Task – Multitasking – Context Switching – Task States – Kernel – Non Preemptive Kernel – Preemptive Kernel – Scheduler – Scheduling Algorithm – Task Priority (static and Dynamic) – Mutual Exclusion – Semaphores – Inter Task Communication – Message Mail Boxes – Message Queues-Introduction – Features of µC/OS –II.	15

Text Book:

1. ARM System-on-Chip Architecture (2nd Edition) by Steve Furber.

2. µC/OS – II The Real Time Kernel by Jean J. Labrosse.

Reference Book:

1. Embedded Systems Architecture – Tammy Noergaard.
2. ARM System Developer's Guide – Andrew N.Sloss.
3. ARM Architecture Reference Manual – David Seal.
4. ARM7TDMI Datasheet
5. Real Time Concepts for Embedded Systems – by Qing Li and Caroline Yao.
6. Embedded / Real Time Systems: Concepts, Design and Programming by Dr. K.V.K.K.Prasad.
7. LPC 2148 User Manual.

MODEL QUESTION PAPER – I

Term : VI Time : 3 Hrs

Programme : Diploma in Electronics and Communication Engg Max Marks : 75

Course : **ELECTIVE THEORY – II** 1. Embedded Systems Code : N1EC407

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART - A

1. Expand ARM 7 TDMI.
2. How many operating states are there in ARM? Mention them.
3. What is the use of Link register?
4. Mention any two features of LPC 2148.
5. What is PCB? Give its use.
6. How many analog inputs are there in LPC 2148? What is the use of ADGSR?
7. Define Kernel. What are the two types?
8. What is multitasking?

PART - B

9. Explain two memory models.
10. Explain AMBA.
11. Name the operating modes in ARM processor.
12. What is the function of wakeup timer?
13. Explain I^2C features.
14. Write about any two ADC registers.
15. Define RTOS. Mention its two types.
16. Explain Context Switching.

[Turn over …..

PART - C

17. (a) Explain about ARM core data flow model.

(OR)

(b) Draw ARM7 functional block diagram and explain each block.

18. (a) Explain ARM7 Pipelining with diagram.

(OR)

(b) Explain about Load/Store instructions in ARM.

19. (a) Explain each block of LPC 2148 Microcontroller with a neat block diagram.

(OR)

(b) Explain about PLL operation in LPC2148 MC.

20. (a) Explain about UART operation in detail.

(OR)

(b) Explain about I^2C operating modes.

21. (a) Explain any two scheduling algorithms in detail.

(OR)

(b) Explain Intertask communication using Semaphore.

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MODEL QUESTION PAPER - II

Term	:	VI	Time	: 3 Hrs
Programme	:	Diploma in Electronics and Communication Engg	Max Marks	: 75
Course	:	**ELECTIVE THEORY – II** 1. Embedded Systems	Code	: N1EC407

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART - A

1. Expand AMBA.
2. Give any two features of ARM.
3. Explain any one Branch instruction in ARM.
4. How many I/O ports are there in LPC 2148?
5. What is the use of ADGSR?
6. How many serial standards are there in LPC 2148? What are they?
7. What is task?
8. Name the two operating states in ARM. How will you switch between two states?

PART - B

9. Explain about Embedded ICE in ARM.
10. Explain about CPSR.
11. Explain about PCB.
12. Explain any two UART registers.
13. Explain about Task States with diagram.
14. Compare RTOS with general OS.
15. Give any three ADC features.
16. Explain about Wake up Timer in LPC 2148.

[Turn over …..

PART - C

17. (a) Explain the internal structure of ARM with neat diagram.

(OR)

(b) With a flowchart explain the software tools for code development in ARM.

18. (a) Explain about Exceptions in ARM.

(OR)

(b) Explain about Data processing instructions in ARM.

19. (a) Explain LPC 2148 block diagram.

(OR)

(b) i) Explain about PLL in LPC 2148.

ii) Explain about VPB Divider.

20. (a) Explain about Timer Registers in LPC 2148.

(OR)

(b) Explain about UART operation in detail.

21. (a) What is Kernel? Explain Non Preemptive Kernel and Preemptive Kernel.

(OR)

(b) What is a scheduler? Explain any two scheduling algorithms in detail.

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N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC408

Term : VI

Course Name : ELECTIVE THEORY – II

2. PROGRAMMABLE LOGIC CONTROLLER

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
ELECTIVE THEORY – II 2. PROGRAMMABLE LOGIC CONTROLLER	Hours / Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topic	Time
1	Architecture and operation of PLC	15
2	Programming of PLC	15
3	PLC Timers and counters	15
4	Advanced instructions	15
5	I/O Module Communication and networking	15
	Total	75

Course Outcomes:

On successful completion of the course, the student will be able to:

C408.1	Familiarize the Architecture and operation of PLC.
C408.2	Developing ladder diagram and Programming the PLC.
C408.3	Familiarize the operation of PLC Timers and counters.
C408.4	Understand and study the Advanced instructions of PLC.
C408.5	Familiarize the I/O Module Communication and networking in PLC.

Course Outcome linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Teaching Hrs.
C408.1	Familiarize the Architecture and operation of PLC.	**R/U/A**	1,2	15
C408.2	Developing ladder diagram and Programming the PLC.	**R/U/A**	2,3	15
C408.3	Familiarize the operation of PLC Timers and counters.	**R/U/A**	4,5	15
C408.4	Understand and study the Advanced instructions of PLC.	**R/U/A**	5	15
C408.5	Familiarize the I/O Module Communication and networking in PLC.	**R/U/A**	5,7	15
		Total sessions		75

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	Architecture and operation of	*15*	25	***2***	***18***	***5***	*17.86*
II	Programming of PLC	*15*	25	***2***	***18***	***5***	*17.86*
III	PLC Timers and counters	15	25	***2***	***18***	***5***	*17.86*
IV	Advanced instructions	15	25	***2***	***18***	***5***	*17.86*
V	I/O Module Communication and	15	25	***2***	***18***	***5***	*17.86*
I to V*			15	***6***	***9***	***0***	*10.70*
	Total	75	**140**	**16**	**99**	**25**	**100**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
ELECTIVE THEORY – II 2. PROGRAMMABLE LOGIC CONTROLLER	**1**	**3**	**1**	**1**	**3**	**-**	**1**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topic	Hours
I	**ARCHITECTURE AND OPERATION OF PLC** Evolution of PLCs – Hard-wired control systems. PLC – definition, features, Advantages, Relays .PLC parts and architecture – CPU – I/O section – Programming device - Memory - input field devices – output field devices – input module wiring connections, output module wiring connections- Power Supply -PLC versus computer - Types of PLC – single ended – multitask – control management- unitary - modular- small – medium – large. Developing circuits from Boolean expression – Hardwired logic to programmed logic – programming word level logic instruction – processor memory organization program files – data files – program scan.	15
II	**PROGRAMMING OF PLC** PLC Programming languages - Standard languages - Ladder diagram (LD) - Function block diagram (FBD) Sequential function chart(SFC)- Statement List(STL) (each one example program)-Symbols of a PLC Input and output contact graphical languages(IES)– program format – Typical Numbering mode – Equivalent ladder diagram of AND, OR, NOT, XOR, NAND AND NOR gate equivalent ladder diagram to demonstrates De Morgan's theorem, Ladder design switches- Develop elementary program design of a 4:1 Multiplexer using ladder logic programming wired level logic instructions input, output, flag, timer, counter, latch.	15
III	**PLC TIMERS AND COUNTERS** Definition and Classification of a timer. Characteristics of a PLC timer – functions in a timer – resetting –retentive functions and function block format- non-retentive – classification – Timer ON-delay- Timer-OFF delay- Simple problems using timer PLC counter – Operation of a PLC counter – Counter parameters – Format of counter instruction and counter data file - count up (CTU)- count down(CTD) simple problems using counter.	15
IV	**ADVANCED INSTRUCTIONS** Introduction - comparison instructions - Addressing format for micro logic system - Different addressing types – Data movement instructions - Mathematical instructions - Program flow control instructions - PID instructions. Program development and execution using PLC. Simplified start up process of a coal feeding to a boiler plant - elevator for 3 floor building - Traffic light control - conveyor belt Selection of PLC - Safety considerations built in the PLC's.	15
V	**I/O MODULE COMMUNICATION AND NETWORKING** Introduction – classification of I/O Module Input – Output system – Direct I/O, parallel I/O – Sourcing and sinking of serial I/O system. PLC interfacing-Discrete Input module –DC - AC – Discrete output module – Analog input module single ended and output module - RTD input modules- Thermocouple - High speed Encoder – Stepper motor- RS-232 interface module-Differential input module. Types of Communication Interface. Parallel – serial – Parallel – IEEE 488 BUS- Serial _ balanced – unbalanced- communication mode- simplex – Half duplex – full duplex features of good interface. Serial interface RS 232c. DB-9 connection of Rs232C Network Topology, Bus Ring, Star, Tree.	15

Text Book :

1. W. Bolton, “Programmable logic controller” IV Edition Reed Elsevier India pvt ltd.
2. Gary Dunning, “Introduction to PLC”, IIIrd edition Thomson del mar learning

Reference Book:

1. Madhuchhanda Mitra ,Samarjit sen Gupta,”PLC and Industrial Automation an introduction”, Penram international Publishing (India) Pvt Ltd.
2. Pradeep Kumar Srivastava, “Exploring Programmable Logic Controller with applications”,
BPB Publication

MODEL QUESTION PAPER - I

Term : VI Time : 3 Hrs

Programme : Diploma in Electronics and Communication Engg Max Marks : 75

Course : Elective Theory – II Code : N1EC408
2. Programmable Logic Controller

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. What is the process of PLC scan?
2. What is programming device?
3. List down the various types of programming a PLC.
4. What is the function of output energise instruction?
5. Give the format of timer instructions?
6. What is the purpose of the instruction CTU?
7. Give the addressing format for micro logic system.
8. What is the use of stepper motor?

PART – B

9. List some standard PLCs available in market.
10. What are the types of PLC?
11. What is the purpose of OTE instruction?
12. Draw the equivalent ladder diagram of XOR gate.
13. Explain the operation of counter in PLCs.
14. Explain the use of data movement instructions.
15. Draw the configuration of sourcing output module.
16. List the advantages of bus topology.

[Turn over …..

PART - C

17. a) Draw and explain the block diagram of PLC system.

(or)

b) (i) What are the applications of PLC?

(ii) Explain the memory organization of standard PLCs.

18. a) State the steps involved in the development of ladder logic diagram. Give one example.

(or)

b) (i) Explain the following instruction : (i) XIO (ii) XIC

(ii) Draw the ladder logic diagram of multiplexer and explain.

19. a) Write and implement a ladder logic program to illustrate the timer operation using TON instruction.

(or)

b) Write and implement a ladder logic program for blinking indicator circuit in which two lights are flashed alternately every 5 seconds using PLC.

20. a) List down the various comparison instructions used in PLC and explain each briefly.

(or)

b) Develop the ladder logic diagram for conveyor belt system and explain the rung in the ladder diagram.

21. a) Explain the function of OUTPUT Modules with neat diagram.

(or)

b) (i) Briefly explain IEEE 488 bus.

(ii) List the advantages and disadvantages of ring topology.

MODEL QUESTION PAPER - II

Term : VI Time : 3 Hrs

Programme : Diploma in Electronics and Communication Engg Max Marks : 75

Course : Elective Theory – II Code : N1EC408
2. Programmable Logic Controller

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART - A

1. Define PLC.
2. What are the advantages of PLC over relay logic?
3. Draw the FDB of multiplexer.
4. What is the function of retentive timer?
5. What is the purpose of the instruction CTD?
6. List the classification of advanced instructions in PLC.
7. Write the type of communication interface.
8. What is the purpose of normally open contact / Examine ON instruction?

PART - B

9. What are the features of PLC?
10. What is the job of CPU in a PLC?
11. List down the basic rules of ladder logic diagram.
12. Draw the equivalent ladder diagram of OR gate.
13. Write about counter parameters.
14. List down the various program flow control instructions.
15. Draw the configuration of sinking output module.
16. List the advantages of ring topology.

[Turn over …..

PART - C

17. a) Draw and explain the detailed block diagram of PLC system.

(or)

b) (i) Explain the working principle of PLC.

(ii) Explain about the additional capabilities of PLC.

18. a) Design ladder logic diagram to implement De-Morgan's theorem.

(or)

b) (i) Explain the following instruction : (i) Output latch (ii) XIC

(ii) Draw the FDB for logic operation AND, OR, NOT.

19. a) Draw a ladder diagram for a two motor system having the following conditions :

(i) The start switch starts motor 1, after motor 1 starts 5 second later motor 2 starts.

(ii) The stop switch stops both motor 1 and motor 2.

(or)

b) Draw and explain the schematic diagram of function block PLC timer.

20. a) List down the various mathematical instructions used in PLC and explain each briefly.

(or)

b) Develop the ladder logic diagram for elevator for three floor building and explain the rung in the ladder diagram.

21. a) Explain the function of INPUT Modules with a neat diagram.

(or)

b) (i) Draw and explain about the star topology.

(ii) List the advantages and disadvantages of bus topology.

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VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1CO400

Term : VI

Course Name : ELECTIVE THEORY II – 3. NANO AND SOLAR ENGINEERING

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
ELECTIVE THEORY - II	Hours / Week	Hours / Term	Marks			Duration
			Internal Assessment	End Examination	Total	
3..Nano and Solar Engineering	5	75	25	75	100	3 Hrs.

Topics and Allocation of Hours:

UNIT	Topics	Hours
I	BASICS OF NANO SCIENCE AND CLASSES OF NANO SCIENCE	15
II	SYNTHESIS, CHARACTERIZATION & APPLICATION OF NANO MATERIAL	15
III	FUNDAMENTALS OF SOLAR CELL AND ITS PERFORMANCE	15
IV	SOLAR CELL CLASSIFICATIONS AND ITS COMPONENTS	15
V	TYPES OF SOLAR SYSTEM AND DESIGN OF SOLAR HOME SYSTEM	15
	TOTAL	**75**

Course Outcomes:

On successful completion of the course, the student will be able to:

C400.1	Understand the basics of Nano technology - properties, behavior and materials
C400.2	Acquire knowledge about synthesis, characterization and applications of Nano material
C400.3	Study about renewable energy sources and understand the basic principle of solar energy conversion
C400.4	Acquire knowledge about the various components of solar cell
C400.5	Able to classify solar system and to design a solar Home system

Course Outcome Linkage to Cognitive level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO,PSO	Teaching Hrs
C400.1	Understand the basics of Nano technology - properties, behavior and materials.	R/U/A	PO1,PSO2	15
C400.2	Acquire knowledge about synthesis, characterization and applications of Nano material.	R/U/A	PO1,PO2,PO4,PSO2	15
C400.3	Study about renewable energy sources and understand the basic principle of solar energy conversion.	R/U/A	PO1,PO5,PSO2	15
C400.4	Acquire knowledge about the various components of solar cell	R/U/A	PO1,PSO2	15
C400.5	Able to classify solar system and to design a solar Home system.	R/U/A	PO1,PO3,PO4,PO7, PSO2	15
		Total sessions		75

Course Content and Blue Print of Marks for End Examination:

Unit No	Unit Name	Hours	Max. Marks	Questions to be set for			Marks weightage (%)
				R	U	A	
I	BASICS OF NANO SCIENCE AND CLASSES OF NANO SCIENCE	**15**	25	***2***	***18***	***5***	*17.86 %*
II	SYNTHESIS, CHARACTERIZATION & APPLICATION OF NANO	**15**	25	***2***	***18***	***5***	*17.86 %*
III	FUNDAMENTALS OF SOLAR CELL AND ITS PERFORMANCE	**15**	25	***2***	***18***	***5***	*17.86 %*
IV	SOLAR CELL CLASSIFICATIONS AND ITS COMPONENTS	**15**	25	***2***	***18***	***5***	*17.86 %*
V	TYPES OF SOLAR SYSTEM AND DESIGN OF SOLAR HOME SYSTEM	**15**	25	***2***	***18***	***5***	*17.86 %*
I to V*			15	***6***	***9***	***0***	*10.70 %*
	Total	75	**140**	**16**	**99**	**25**	**100 %**

*** 3 x 2Marks and 3 x 3Marks from any Unit limited to maximum of 2 Questions in each unit**

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
ELECTIVE THEORY - II 3..Nano and Solar Engineering	3	2	3	3	2	-	1

Course-PSO Attainment Matrix:

Course Name	Programme Specific Outcomes	
	1	2
ELECTIVE THEORY - II 3..Nano and Solar Engineering	-	3

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

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- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

N1CO400 – NANO AND SOLAR ENGINEERING

DETAILED SYLLABUS

Contents: Theory

Unit	Name of the Topics	Hours
I	**BASICS OF NANO SCIENCE AND CLASSES OF NANO SCIENCE** Nano technology – Difference between bulk and Nano scale materials – Properties at the Nano scale –Size dependent behavior. Quantum dots – Nano wells – Nano films and Nano wires – Bucky balls – Carbon Nano tubes – Single walled and Multi walled CNT.	**15**
II	**SYNTHESIS, CHARACTERIZATION AND APPLICATION OF NANO MATERIAL** Top-Down approach – Nanolithography – Ball Milling - Bottom-Up approach – CVD (Chemical Vapor Deposition). Sol-gel processing – Spin Coating Method, Dip Coating Method. Characterization of Nano Particles - SEM –XRD – UV Spectroscopy, PV Characteristics of Nano Thin Films using 4 probe methods. Hydrophobic nature of Nano Thin films. Application of Nano Technology - Electronics – Textiles – Solar technology – Construction Materials –Nano Technology in medical science – Drug Delivery system for Cancer Treatment.	**15**
III	**FUNDAMENTALS OF SOLAR CELL AND ITS PERFORMANCE** **Energy Resources:** Renewable energy sources scenario in India – Importance of renewable energy sources-Wind energy-Solar energy-Advantages of solar energy - Physics of the Sun - Solar spectrum - green house effect **Concepts:** Photovoltaic effect - Principle of direct solar energy conversion into electricity in a solar cell -Solar cell, p-n junction – structure - I-V characteristics - effect of irradiation and temperature - fill factor - maximum power point – losses - cell efficiency	**15**

IV	**SOLAR CELL CLASSIFICATIONS AND ITS COMPONENTS** Types of Solar cells - Solar Modules - Blocking Diode - By-pass Diode - Solar Array - Isolation Diode – **Batteries in Solar PV Systems:** Battery Types and Classifications, Construction of Lead – Acid battery, Lead-Acid Battery Chemistry, Modern Rechargeable Batteries, Methods of Battery Charging **Charge controllers**: Shunt regulator, Series regulator, Methods of Charging the Battery by CR. **Inverters:** Basic Principle of operation, Types of Inverters.	**15**
V	**TYPES OF SOLAR SYSTEM AND DESIGN OF SOLAR HOME SYSTEM** **Classification:** Stand alone PV system - Grid connected PV System - Hybrid solar PVsystem **Design of Solar Home System (SHS)** - Selection of Solar PV module - Selection of Battery - Selection of Charge Controller - Selection of DC/AC Inverter - Selection of DC/DC converter - Selection of switch - Selection of the wire size for solar home system	**15**

Text Books:

1. "Nano Technology" – N.Arumugam, SaraS Publication.
2. Pradeep.T, Fundamentals of Nanoscience and Nanotechnology, Mc GrawHill,2012.
3. Sukhatme .S.P, Nayak .J.K, "*Solar Energy",* Tata McGraw Hill Education Private Limited, New Delhi, 2010.
4. Unit III to Unit V *Training Manual For Engineers on Solar PV System* published by Government of Nepal, Ministry of Environment, Science and Technology.
5. Solar photovoltaic systems technical training manual by Herbert A Wade UNESCO publishing.

Reference Books:

1. C.P.Poole, Jr. Frank J.Owens, Introduction to Nanotechnology (Wiley India Pvt. Ltd.).
2. S.K. Kulkarni, Nanotechnology: Principles & Practices (Capital PublishingCompany).
3. K.K. Chattopadhyay and A.N. Banerjee, Introduction to Nanoscience & Technology
4. (PHI Learning Private Limited).
5. Chetan Singh Solanki., *Solar Photovoltaic: "Fundamentals, Technologies and Application",* PHI Learning Pvt., Ltd., 2009.
6. John R. Balfour, Michael L. Shaw, Sharlave Jarosek*., "Introduction to Photovoltaics",* Jones & Bartlett Publishers, Burlington, 2011.

MODEL QUESTION PAPER - I

Term : VI Time : 3 Hours

Programme : Diploma in Electronics and Communication Engineering Max. Marks: 75

Course : Elective Theory - II 3.Nano and Solar Engineering Code : N1CO400

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. What is Nano technology?
2. Write notes on fullerene.
3. What is top down approach?
4. What is SEM?
5. What is a renewable energy source?
6. What is photo voltaic effect?
7. Name the types of inverter.
8. What is a Hybrid PV system?

PART – B

9. Explain about nano wires.
10. Briefly explain spin coating method.
11. Write the applications of nano technology in medicine.
12. Explain I-V characteristics of PV cells
13. Write the advantages of solar energy.
14. Explain Blocking diode with block diagram.
15. Explain with Block diagram Stand alone PV System.
16. What are the factors to be consider while design a stand alone PV system?

[Turn over …..

PART – C

17. (a). i. Discuss the difference between nano and bulk materials.

ii. Write short notes on size dependant behavior of nano materials.

(Or)

(b). Explain Single walled and multi walled CNT.

18. (a). What is Top down approach? Explain any one method with neat sketch.

(Or)

(b). Explain about SEM with block diagram.

19. (a). Draw the different types of wind turbines and explain. Write the advantages and disadvantages of wind energy.

(Or)

(b). Explain the process of converting Solar energy into electric energy in a PV cell.

20. (a). Explain about the construction of a Lead acid battery.

(Or)

(b). Explain the various methods of charging a battery by CR.

21. (a). Explain with block diagram the Working of Grid connected PV system.

(Or)

(b). Explain the design procedure for Solar Home system.

MODEL QUESTION PAPER - II

Term : VI Time : 3 Hours

Programme : Diploma in Electronics and Communication Engineering Max. Marks : 75

Course : Elective Theory - II 3.Nano and Solar Engineering Code : N1CO400

[N.B: (1) Answer any FIVE Questions in each PART – A and PART – B. Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory.

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 Marks in PART – A, 3 Marks in PART – B and 10 Marks in PART – C.]

PART – A

1. What is Nano material?
2. Write notes on bucky ball.
3. What is bottom up approach?
4. What is XRD?
5. What is a non renewable energy source?
6. What is about Voc in solar cell.
7. What is secondary cell?
8. What is a standalone PV system?

PART – B

9. Define Fullerene.
10. Define CNT.
11. What is CVD process?
12. Write the applications of nano technology.
13. Write the advantages of Wind energy.
14. Draw the IV characteristics of solar cell.
15. What is Bypass diode?
16. Write the formula for finding solar panel capacity.

[Turn over …..

PART – C

17. (a). i. Discuss the difference between nano and bulk materials.

ii. Write short notes on Quantum dots.

(Or)

(b). Explain in detail about Carbon Nano Tube and its types.

18. (a). What is Bottom Up approach? Explain any one method with neat sketch.

(Or)

(b). Explain about the applications of nano technology.

19. (a). Draw and explain the different types of wind turbines.

(Or)

(b). Explain about P-N Junction in detail.

20. (a). Explain about Blocking diode and Bypass diode in detail.

(Or)

(b). Explain the basic principle of operation of inverters.

21. (a). Explain briefly about the types of solar PV system.

(Or)

(b). Design a Solar home system for the given AC load profile

Load profile of the SHS user

Particular	Quantity	Power (Watt)	Daily operation (Hours)	Remarks
Electric lamp	1	10	3	Living room
Electric lamp	1	7	3	Kitchen
Total		17		

VIRUDHUNAGAR S.VELLAICHAMY NADAR POLYTECHNIC COLLEGE (AUTONOMOUS)

(Affiliated to Directorate of Technical Education, Chennai-25)

VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme **: Diploma in Electronics and communication Engineering**

Course code **: N1EC314**

Term **: VI**

Course Name **: Computer Hardware Servicing and Networking Practical**

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
Computer Hardware Servicing and Networking Practical	Hours / Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C314.1	Install and configure the Scanner, Webcam, Biometric device, DVD and Blu-ray Writer
C314.2	Perform Assembling and Dissembling of Laptop and Mobile phones
C314.3	Install and test computer networking and sharing of resources.
C314.4	Identify faults and troubleshooting of various parts of Mobile Phones.

Course Outcome linkage to Cognitive Level:

On successful completion of the course, the students will be able to attain following Course Outcomes

Course Outcome		Experiment linked	CL	Linked PO	Teaching Hrs
C314.1	Install and configure the Scanner, Webcam, Biometric device, DVD and Blu-ray Writer	1,2,3,4	U,A	1,4	20
C314.2	Perform Assembling and Dissembling of Laptop and Mobile phones	5,6,13	U,A	1,4	15
C314.3	Install and test computer networking and sharing of resources.	7,8, 9,10,11,12	U,A	2,4	30
C314.4	Identify faults and troubleshooting of various parts of Mobile Phones.	14,15	U,A	2,4,5	10
			Total sessions		**75**

Legends: R = Remember U= Understand; A= Application and above levels (Bloom's revised taxonomy)

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
Computer Hardware Servicing and Networking Practical	**3**	**3**	**-**	**3**	**1**	**--**	**--**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

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LIST OF EXERCISES

1. Identification of System Layout
   i) Identify front panel indicators & switches and Front side & rear side connectors
   ii) Familiarize the computer system layout by marking positions of SMPS, Motherboard, FDD, HDD, CD,DVD and add on cards.
2. DVD/BLU-RAY WRITER:
   i) Install and Configure a DVD Writer and record a blank DVD.
   ii) Install and Configure a Blu-ray Writer and record a blank Blu-ray Disc
3. Install and configure SCANNER, and WEB CAM
4. Install and configure LASER Printer and Bio-metric device.
5. (i)Assemble and Disassemble a Laptop to identify the parts.
   (ii)Install OS in the Laptop.
6. Installation of OS in the assembled system
   (i) Configure bios setup program and troubleshoot the typical problems using BIOS utility
   (ii) Install, Configure, Partition and Format Hard disk.
   (iii) Installing operating System.
7. Do the following Cabling works for establishing a network
   i)Crimp the network cable with RJ 45 connector in Standard cabling mode.
   (ii)Crimp the network cable with RJ 45 connector in cross cabling mode.
   (iii) Test the crimped cable using a cable tester.
8. Use IPCONFIG, PING, TRACERT and NETSTAT utilities to debug the network issues.
9. Interface two PCs to form Peer To Peer network using the connectivity devices Switch or Router in a LAN.
10. i) Share the files and folders in a LAN.
    ii) Share a printer in a LAN.
11. Configure DNS to establish interconnection between systems and describe how a name is mapped to IP Address.
12. i)Install and configure Network Devices: HUB, Switch or Routers
    ii)Install and Configure NIC.
13. Assembling and Disassembling of Mobile Phones.
14. Fault finding and troubleshooting of Ear piece, Microphone, Keypad and Display Sections of Mobile Phones.
15. Flashing, Unlocking and Formatting memory cards in Mobile phones.

STUDY EXPERIMENTS (Not for Examination)

1. Android applications for mobile phones and Installation of Mobile OS.
2. Install Dual OS in assembled system.

LIST OF EQUIPMENTS

EQUIPMENTS/ SOFTWARES REQUIRED:

Sl. No.	Name of the Equipments	Required Nos.
13.	Computer with Pentium / Core processors with inbuilt NIC	30
14.	CDD/ DVD Writer	02
15.	Blank Blu-ray disk	30
16.	Web camera	02
17.	Blank DVD	30
18.	Scanner	02
19.	Laptop	02
20.	Bio metric device	02
21.	Crimping Tool	02
22.	RJ45 Tester	02
23.	Modem with internet connection	02
24.	Hub	02
25.	Switch/ Router	02
26.	Android Mobiles	02
27.	Keypad Mobile	01
28.	Network Cables	As required

SOFTWARE REQUIREMENTS:

Sl. No.	Name of the Software
1.	Windows XP operating system/ Windows 7 OS
2.	DVD/ CD Burning S/W (Ahead Nero or latest S/W)

Detailed Allocation of Marks for External Assessment

Scheme of valuation in TEE		
1.	Procedure	20
2.	Execution	30
3.	Result & Printout	20
4.	Viva-voce	5
	Total	**75**

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VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC315

Term : VI

Course Name : PCB Design Practical

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
PCB Design Practical	Hours / Week	Hours / Term	Marks			Duration
	5	75	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C315.1	Understand steps involved in schematic, layout, fabrication.
C315.2	Design (schematic and layout) PCB for analog circuits.
C315.3	Design (schematic and layout) PCB for, digital circuits.
C315.4	Design (schematic and layout) PCB for mixed circuits.

Course Outcome linkage to Cognitive Level:

On successful completion of the course, the students will be able to attain following Course Outcomes

Course Outcome		Experiment linked	CL	Linked PO	Teaching Hrs
C315.1	Understand steps involved in schematic, layout, fabrication	1,2,3	R,U,A	1,2,3,4	15
C315.2	Design (schematic and layout) PCB for analog circuits,	4,5,11,12	U,A	2,3,4	20
C315.3	Design (schematic and layout) PCB for, digital circuits	7,8,9,10	U,A	2,3,4	20
C315.4	Design (schematic and layout) PCB for mixed circuits.	6,13,14,15	U,A	3,4	20
			Total sessions		75

Legends: R = Remember U= Understand; A= Application and above levels (Bloom's revised taxonomy)

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
PCB DESIGN PRACTICAL	**1**	**3**	**3**	**3**	**-**	**-**	**-**

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LIST OF EXERCISES

Design the Experiments (Single side PCB ONLY) using Any EDA tools like TINA, MultiSim , ORcad.

1. Design PCB for Full wave rectifier.
2. Design PCB for Bridge rectifier.
3. Design PCB for CE or CB or CC Amplifier circuits using discrete components.
4. Design PCB for Amplitude Modulator.
5. Design PCB for Frequency Modulator.
6. Design PCB for Astable Multivibrator using 555 IC.
7. Design PCB for half adder using Logic gates.
8. Design PCB for full adder using Logic gates.
9. Design PCB for 4 bit binary counter using D Flip Flops.
10. Design PCB 4 bit shift Register (PIPO) using JK Flip Flops.
11. Design PCB for Positive Voltage Regulator using 7805 & 7812 IC.
12. Design PCB for Analog Multiplier using 741 IC.
13. Design PCB for flashing LEDs using 555 IC.
14. Design PCB for Fan Regulator.
15. Design PCB for Liquid Level Controller.

LIST OF EQUIPMENTS

HARDWARE REQUIREMENT:

Desktop / Laptop Computers : 15 Nos.
Laser Printer : 1 Nos.

SOFTWARE REQUIREMENT:

PCB Design software like (Any EDA tools like TINA, MultiSim, ORcad)

Detailed Allocation of Marks for External Assessment

SCHEME OF VALUATION IN TEE		
1.	CONSTRUCTION & PROCEDURE	30
2.	IMPORT & PREPARATION	10
3.	PCB LAYOUT	20
4.	OUTPUT	10
5.	VIVA-VOCE	05
	Total	**75**

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VIRUDHUNAGAR – 626 001

N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC409

Term : VI

Course Name : ELECTIVE PRACTICAL – I

1. EMBEDDED SYSTEMS PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
ELECTIVE PRACTICAL – I	Hours / Week	Hours / Term	Marks			Duration
1. EMBEDDED SYSTEMS PRACTICAL	4	60	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C409.1	Write assembly language program for arithmetic operations.
C409.2	Write Embedded C Program for relay, buzzer, LEDs and stepper motor interface.
C409.3	Write Embedded C Program for ADC, Keypad, Serial port and LCD interface.
C409.4	Write Embedded C Program for RTC and Seven segment display interface through I^2C.

Course Outcome linkage to Cognitive Level:

On successful completion of the course, the students will be able to attain following Course Outcomes

Course Outcome		Experiment linked	CL	Linked PO	Linked PSO	Teaching Hrs
C409.1	Write assembly language program for arithmetic operations.	1, 2	R, U	1, 2	1,2	8
C409.2	Write Embedded C Program for relay, buzzer, LEDs and stepper motor interface.	3, 4, 5, 6, 7	R, U, A	2, 3	2	20
C409.3	Write Embedded C Program for ADC, Keypad, Serial port and LCD interface.	8, 9, 10, 11, 12	R, U, A	2, 3	2	20
C409.4	Write Embedded C Program for RTC and Seven segment display interface through I^2C.	13, 14	R, U, A	2, 3, 4, 5, 7	2	12
			Total sessions			**60**

Legends: R = Remember U= Understand; A= Application and above levels (Bloom's revised taxonomy)

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
ELECTIVE PRACTICAL – I 1. EMBEDDED SYSTEMS PRACTICAL	**1**	**3**	**3**	**1**	**1**	**-**	**1**

Course-PSO Attainment Matrix:

Course Name	Programme Specific Outcomes	
	1	2
ELECTIVE PRACTICAL – I 1. EMBEDDED SYSTEMS PRACTICAL	**1**	**3**

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LIST OF EXERCISES

1. Write Simple Assembly Language Programs for
   a. Addition b. Subtraction and execute it.

2. Write Simple Assembly Language Programs for
   a. Multiplication b. Division and execute it.

3.Write Embedded C Program for 8 bit LED Interface and execute it.

4.Write Embedded C Program for Buzzer Interface and execute it.

5.Write Embedded C Program for Relay Interface and execute it.

6.Write Embedded C Program for Switch & LED Interface and execute it.

7.Write Embedded C Program for Stepper Motor Interface and execute it.

8.Write Embedded C Program for Serial communication (UART0) and execute it.

9.Write Embedded C Program for Analog to Digital Conversion (On chip ADC) and execute it.

10.Write Embedded C Program to interface with LM35 Temperature sensor and execute it.

11.Write Embedded C Program for 4 × 4 Matrix Keypad Interface and execute it.

12.Write Embedded C Program for LCD Interface and execute it.

13.Write Embedded C Program for Seven Segment LED Display Interface through I^2C and execute it.

14.Write Embedded C Program for RTC.

LIST OF EQUIPMENTS

EQUIPMENTS / COMPONENTS REQUIRED

Sl. No.	Name of the Equipments	Required Nos.
1.	LPC 2148 Microcontroller Kit	9
2.	Stepper Motor	2
3.	LM35 Temperature sensor	2

Detailed Allocation of Marks for External Assessment

SL. No.	DESCRIPTION	MAX. MARK
1.	Program Writing	35
2.	Debugging and Execution	30
3.	Result	05
4.	Viva-Voce	05
	Total	**75**

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VIRUDHUNAGAR – 626 001

N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC410

Term : VI

Course Name : ELECTIVE PRACTICAL – I

2. PROGRAMMABLE LOGIC CONTROLLER PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
ELECTIVE PRACTICAL – I 2. PROGRAMMABLE LOGIC CONTROLLER PRACTICAL	Hours / Week	Hours / Term	Marks			Duration
	4	60	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C410.1	Draw the ladder diagram for PLC
C410.2	Interface switches with PLC
C410.3	Apply PLC in simple applications
C410.4	Apply PLC in Real Time Applications

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		Linked Expts.	CL	Linked PO	Teaching Hrs
C410.1	Draw the ladder diagram for PLC	**1,2,3**	R,U	1	12
C410.2	Interface switches with PLC	**4,5,6,7**	R,U	2,3,4	16
C410.3	Apply PLC in simple applications	**8,9,10,11**	U,A	5,6,7	16
C410.4	Apply PLC in Real Time Applications	**12, 13,14,15**	U,A	5,6,7	16
		Total sessions			**60**

Legends: R = Remember U= Understand; A= Application and above levels (Bloom's revised taxonomy)

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
Elective Practical – I 2. Programmable Logic Controller Practical	**1**	**1**	**1**	**1**	**3**	**3**	**3**

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LIST OF EXERCISES

1. Write and implement a simple ladder logic program using digital inputs and outputs for PLC.
2. Write and implement a simple ladder logic program using timer in PLC.
3. Write and implement a simple ladder logic program using counter in PLC.
4. Interfacing of Limit switch with PLC.
5. Interfacing of Reed switch and Proximity switch with PLC.
6. DOL starter with single phase prevention.
7. EB to Generator Change over switch implementation with interlocking.
8. Fill the water in water tank and maintain the water level using PLC.
9. Fire alarm control using PLC.
10. Three floor Lift control using PLC.
11. Traffic light control using PLC.
12. Heater control using PLC.
13. Round table liquid filling system using PLC.
14. Slow speed motor control using PLC.
15. Conveyor belt control using PLC.

LIST OF EQUIPMENTS

Sl. No.	Name of the Equipments	Required Nos.
1.	PLC suitable to conduct above experiments	3
2.	Limit switch	1
3.	Reed switch	1
4.	Inductive proximity sensor	1
5.	Capacitive proximity sensor	1
6.	PC laptop	3

Detailed Allocation of Marks for External Assessment

SL. No.	DESCRIPTION	MAX. MARK
1.	Circuit Diagram	25
2.	Connection	20
3.	Execution	15
4.	Result	10
5.	Viva-Voce	05
	Total	**75**

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VIRUDHUNAGAR – 626 001

N1 - SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1CO401

Term : VI

Course Name : ELECTIVE PRACTICAL - I

3. NANO AND SOLAR ENGINEERING PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
ELECTIVE PRACTICAL - I 3. Nano and Solar Engineering Practical	Hours / Week	Hours / Term	Marks			Duration
	4	60	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

C401.1	**Synthesis and Characterization of Nano material**
C401.2	**Measure various parameters for understanding PV cell performance**
C401.3	**Calculate MPP and power flow in AC and DC load**

Course outcome Linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		Linked Expts.	CL	Linked PO,PSO	Teaching Hrs
C401.1	Synthesis and Characterization of Nano material	1,2,3,4,5,6	U/A	PO1,PO2,PO4 PSO2	24
C401.2	Measure various parameters for understanding PV cell	7,8,9,10,11 ,12,13	U/A	PO1,PO2,PO4 PSO2	24
C401.3	Calculate MPP and power flow in AC and DC load	14,15,16	U/A	PO1,PO2,PO4 PSO2	12

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
3. Nano and Solar Engineering Practical	**3**	**3**	**-**	**3**	**-**	**-**	**-**

Course-PSO Attainment Matrix:

Course Name	Programme Specific Outcomes	
	1	**2**
3. Nano and Solar Engineering Practical		3

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

- *If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3*
- *If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2*
- *If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1*
- *If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.*

LIST OF EXPERIMENTS

PART – A

LIST OF NANO LAB EXPERIMENTS

1. Preparation of Nano particles using Ball Mill.
2. Synthesis of Nano thin film on one side of substrate by Spin coating method.
3. Synthesis of Nano thin film on two sides of substrate by Dip coating method.
4. Measurement of Nano film thickness using Spectroscopic reflectometer.
5. Measurement of VI Characteristics of Nano film.
6. Comparison of Hydrophobic Characteristics of Natural and Synthetic Nano Materials.

PART – B

LIST OF SOLAR LAB EXPERIMENTS

7. Measurement of Solar Radiation using Solarimeter and Lux Meter.
8. I-V and P-V Characteristics of PV module with varying radiation.
9. I-V and P-V Characteristics of series connection of PV modules.
10. I-V and P-V Characteristics of parallel connection of PV modules.
11. Effect of variation in tilt angle on PV module power.
12. Effect of Shading on the output of Solar panel.
13. Working of diode as blocking diode.
14. Power flow calculation of standalone PV system of AC load with battery.
15. Power flow calculation of standalone PV system of DC load with battery.
16. Find the MPP manually by varying the resistive load across the PV panel.

PART – C

1. *Study the operation of a windmill* ***(Not for examination)***

LIST OF EQUIPMENTS

NANO ENGINEERING

1	Muffle Furnace
2	Magnetic Stirrer
3	Ultra Sonicator
4	Spin Coating Machine
5	Dipping Machine
6	Spectroscopic Reflecto meter
7	Four Probe Method
8	Contact Angle Meter
9	Digital Weighing Machine
10	Double Distillation Water Still
11	Ball Mill

SOLAR ENGINEERING

1	Solar panel PV training system	6
2	Infra-red Thermometer	1
3	Luxmeter	2
4	Solar power meter	1
5	Solar Panel 100W(Mono – 1, Poly – 2)	3
6	Inverter (PWM, MPPT – each 1 No.)	2
7	Battery	1
8	Charge Controller 12V / 10A	2
9	DC Voltmeter (MECO make)	6
10	DC Ammeter (MECO make)	6
11	AC / DC Digital tong tester	2
12	Rheostat	1

END EXAMINATION

Note: All the exercise should be given in the question paper and students are allowed to

select by lot. (Nano or Solar)

Detailed Allocation of Marks for External Assessment

Procedure	30 marks
Sketches/Circuit diagram	10 marks
Tabulation	10 marks
Calculation/graph	10 marks
Result	10 marks
Viva – voce	05marks
TOTAL	**75 marks**

VIRUDHUNAGAR S.VELLAICHAMY NADAR POLYTECHNIC COLLEGE (AUTONOMOUS)

(Affiliated to Directorate of Technical Education, Chennai-25)

VIRUDHUNAGAR – 626 001

N1 – SCHEME

Programme : Diploma in Electronics and Communication Engineering

Course code : N1EC316

Term : VI

Course Name : Project Work and Seminar

TEACHING AND SCHEME OF EXAMINATION

Number of weeks per Term: 15 weeks

Course	Instructions		Examination			
Project Work and Seminar	Hours / Week	Hours / Term	Marks			Duration
	4	60	Internal Assessment	End Examination	Total	
			25	75	100	3 Hrs.

Course Outcomes:

On successful completion of the course, the student will be able to:

Code	**Course Outcome**
C316.1	Have an exposure to an innovative area of technology/Information.
C316.2	Develop presentation skills.
C316.3	Develop creative interaction among listeners.
C316.4	Develop prototype/model of a product
C316.5	Enhance team spirit and creative talents for achieving a goal.
C316.6	Implement the theoretical and practical knowledge gained through the curriculum into an application suitable for a real practical working environment perfectly in an industrial environment.
C316.7	Communicate with experts and the community and use their knowledge in developing the project.
C316.8	Analyze the design of the project to ensure it meets the specifications (validate its operational viability)

Course Outcome linkage to Cognitive Level:

Cognitive Level Legend: R- Remember, U- Understand, A- Application

Course Outcome		CL	Linked PO	Teaching Hrs
C316.1	Have an exposure to an innovative area of technology/Information.	**R/U/A**	2, 7	6
C316.2	Develop presentation skills.	**R/U/A**	6	3
C316.3	Develop creative interaction among listeners.	**R/U/A**	6	3
C316.4	Develop prototype/model of a product	**R/U/A**	3, 6, 7	9
C316.5	Enhance team spirit and creative talents for achieving a goal.	**R/U/A**	6	3
C316.6	Implement the theoretical and practical knowledge gained through the curriculum into an application suitable for a real practical working environment perfectly in an industrial environment.	**R/U/A**	1 , 2, 3, 4, 6, 7	15
C316.7	Communicate with experts and the community and use their knowledge in developing the project.	**R/U/A**	5, 7	6
C316.8	Analyze the design of the project to ensure it meets the specifications (validate its operational viability)	**R/U/A**	3, 5, 6, 7	15
		Total sessions		60

Course-PO Attainment Matrix:

Course Name	Programme Outcomes						
	1	2	3	4	5	6	7
Project Work and Seminar	**1**	**2**	**3**	**1**	**2**	**3**	**3**

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Seminar topics:-

Human values
Integrity
Changing attitude
Self-Confidence
Spirituality
Safety and risk
Responsibility of engineers
Types of responsibility
Environmental Ethics
Plastic waste disposal
E-waste disposal
Semi conductor waste disposal
Industrial waste disposal
Human rights
Human rights of woman
Status of woman in India
National Human Right commission constitution
Intellectual property Right

Internal Assessment :-

The internal assessment should be calculated based on the review of the progress of the work done by the student periodically as follows.

Detail of assessment	Period of assessment	Maximum marks
First Seminar	3rd week	2.5
First Review	4th week	05
Second seminar	9th week	2.5
Second review	10th week	05
Attendance		05
Report		05
	Total	25

Project Review I & II (VI Terms) (5 + 5) :10 Marks
Seminar I & II (5 + 5) = 10 / 2 : 5 Marks
Attendance : 5 Marks
Report : 5 Marks
Total :25 Marks

End Examination

Composition of Educational Components:

Minimum marks for pass is 50 out of which minimum 35 marks should be obtained out of 75 marks in the board examinations alone.

Detailed Mark Allocation for End Examination for Project work:-

S.No	Criteria Component	MARKS
1	Relevance of topic	10
2	Knowledge of methodology	20
3	Role of individual in the team	10
4	Finding of the study	10
5	Viva-voce	25
TOTAL		75